WANG LABORATORIES, INC.

TO: Telecommunication Development Groups

FROM: R. M. Marston/Hsin Lin

DATE: May 21, 1981

SUBJECT: Changes to Telecommunications Processor (TCB-1) Specifications
ADDENDUM to HM 28

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1. Section 2.17 (changes)

Address X '34' Control Register/"Deadman" Timer Control

Address X '35' Base Register, Monitor Block/Character Table

2. Section 12.2 (changes)

NB1, NB2, NB4, NB8, DPR, CRQ are active "low". (on = "ϕ" off = "1")

ACR, PND, PWI, COS, DOL, RI, TM, MPE, ZERO, SF/RF are active "high". (on = "1" off = "0")

3. Section 6.3 (addition)

The non-maskable interrupt (NMI) to the Z80 CPU is sourced from either the "Deadman timer" (ENMI see figure A) or "Latched Memory Parity Error" (LMPE see figure B). The selection of which source is accomplished by means of physical jumpers.

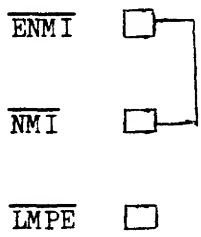

Figure A

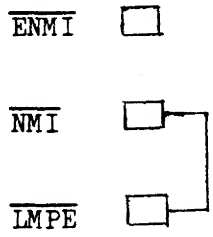

Figure B

0011E

T E C H N I C A L M E M O R A N D U M

H M 2 8

TO: Telecommunication Development Groups

FROM: Roger Cross

DATE: December 1, 1980

RE: Telecommunication Processor (TCB-1)

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INTRODUCTION

TELECOMMUNICATION PROCESSOR

Ø.1 Telecommunications for the Wang Systems will encompass a wide range of line disciplines and link protocols. To further this end, the TCB-1 Telecommunication Processor utilizes the following LSI components:

Z8ØA-CPU (4MHz clock operation), Z8ØA-SIO/2, Z8ØA-CTC, 9517A-DMA Controller (2MHz clock operation), and up to 64K bytes of Random Access Memory (MK4116-3).

Ø.2 The TCB-1 will also utilize a number of MSI components to provide:

928 Data Link; Power On Diagnostics; Memory Parity control; RS-232-C, and RS-449 MODEM interfaces; RS-366 Automatic Calling Unit interface; Character Recognition interrupts; 928 Data Link memory write access monitor; "Deadman" timer; and a TCB-1 Status Display panel.

PREREQUISITES

Ø.3 The following manuals and data sheets are required reading:

1) Z8ØA-CPU Technical Manual
2) Z8ØA-SIO Technical Manual
3) Z8ØA-CTC Technical Manual
4) AM9517A Direct Memory Access Controller
5) OIS System Operation OS-6
6) EIA Standard RS-232-C
7) EIA Standard RS-449
8) EIA Standard RS-366

Ø.4 Several other OIS System documents (TM documents) would be useful but are not required to understand this description.

GENERAL DESCRIPTION

1.Ø The Telecommunication Processor, hereafter referred to as the TCB-1, provides the flexibility to support almost any protocol and line discipline. The TCB-1 functional groups are a Processor section, Memory Controller section, and the 928 Data Link section. The Processor section contains the Z8ØA-CPU; Z8ØA-SIO/2; Z8ØA-CTC; RS-232-C, RS-449 and RS-366 interfaces; 9517A-DMA Controller; Character/928 Data Link (Master) monitor; "Deadman" timer; and TCB-1 Status display. The 928 Data Link section contains the coaxial line receive/transmit control, instruction and status/error control, and memory address/data control. The Memory Controller section coordinates TCB-1 memory access between the Processor section and the 928 Data Link section.

Processor Section

1.1 The central processing element, CPU, operates on a 25Ø.4 ns clock cycle. The CPU and the DMA Controller share a common bus, and use Bus Request/Bus Acknowledge to synchronize exchange of the bus control. Note: The DMA Controller operation will slow the Z8ØA-CPU execution, approx. 2 microseconds per byte.

1.2 The SIO/2 is controlled by the CPU and/or the DMA Controller; DMA allows very high speed communications (up to 88ØK bits per second) with minimal system overhead.

1.3 A CTC provides: a BAUD rate clock, a timer, and DMA Controller completion interrupts.

1.4 The communication interface allows either RS-232C or RS-449, program selectable, MODEM connections. The line encoding may be standard NRZ or NRZI, program selectable. The RS366 interface, standard for Automatic Calling Units (ACU), allows the TCB-1 to originate a communication session.

1.5 The Character/Master monitor enables the TCB-1 to monitor memory write accesses of the SIO/DMA and/or the 928 Data Link.

The monitor contains 1Ø24 (1K) bytes of Vector memory, which is shared between the Character and Master monitor functions.

1.6 The Character monitor allows the TCB-1 to conditionally generate a specific vectored interrupt if a program specified character is deposited by the DMA controller. The Character monitor uses a character recognition vector tables of 256 bytes in length. The system software may select any one of four vector tables to allow rapid context switching while processing a received data stream. The deposited character is used as an address to perform a "Lookup" in the program selected vector table. If the byte retrieved from the table has an LSB (VØ) of Ø, or the Monitor Control INTALL is on (see 9.7), an interrupt will be generated using this byte to form the Character vector. The Character Vector will always have V7 = 1 and VØ = Ø.

1.7 The Master monitor allows the TCB-1 to conditionally generate a specific vectored interrupt if a program specified memory address is written by 928 Data Link. The TCB-1 can monitor any 1k memory block, hereafter called the Monitor block, aligned on a 1k address boundary. The address (AØ-A9) in the Monitor block is used to retrieve a byte from Vector memory, if the MSB (V7) = Ø an interrupt will be generated using the retrieved byte to form the interrupt vector. The Master Vector will always have V7 = Ø and VØ = Ø.

1.8 The "Deadman" timer insures that the TCB-1 will not "Hang" the communications line in the event of a hardware/software fault. The timer will force Request To Send (RTS) into the inactive state if not reset by the system software every Ø.5 seconds or less. The timer may optionally force the CPU into the Non-Maskable interrupt service routine at location X'ØØ66' if the timer expires.

1.9 The Status Display provides signaling to a front mounted Light Emitting Diode (LED) display, this allows a varity of conditions to be displayed to the system operator.

928 Data Link Section

1.1Ø The 928 Data Link utilizes a dual coaxial cable to convey control and data information between the 928 Master and Slave Data Links. The channel, operated in half-duplex balanced mode, utilizes a high speed (4.275 M bits per second) START/STOP line discipline. The line format consists of eleven bit words containing: a Start bit, eight Data bits (SØ-S7), a Parity bit, and a Stop bit. The 928 Slave Data Link, under control of the Master Data Link (hereafter reffered to as "Master"), can respond to six different commands: two control commands, and four memory access commands. A summary follows:

928 Data Link Commands

1.11

Command	Action
RESTART	instructs 928 Data Link to RESET the Processor, clear IPL, MPE, and exit, if not already, Diagnostic mode
STATUS	instructs 928 Data Link to transmit the 928 Data Link and Processor status (CPE, IPL, MPE, etc.)
READ1	instructs 928 Data Link to transmit to the Master one byte from the specified TCB-1 memory address
WRITE1	instructs 928 Data Link to receive from the Master one byte and deposit it at the specified TCB-1 memory address
READ256	instructs 928 Data Link to retrieve from TCB-1 memory and transmit to the Master 256 bytes of data starting at the specified 256 byte aligned address
WRITE256	instructs 928 Data Link to receive from the Master 256 bytes of data and deposit it at the specified 256 byte aligned TCB-1 memory address

Memory Controller Section

1.12 The Memory Controller section coordinates memory access to TCB-1 memory. The memory space, organized as 8 bit bytes, may range between 16K and 64K bytes in 16K byte increments. The Memory Controller monitors requests from the 928 Data Link section and the Processor section on a round robin basis. Memory request are either granted by a READY notification or pended by a WAIT notification, thus allowing Processor and 928 data Link access interleaving. Note: 928 Data Link accesses will slow Processor execution. During a 256 byte page transfer, average reduction in Processor speed is 30%.

CPU Functions

2.0 The CPU is the main control and processing element of the TCB-1. Under direction of the system software, the CPU controls all functions of the TCB-1 except the 928 Data Link. The 928 Data Link, controlled by a Data Link Master, controls the Reset (RST), Initial Program Load (IPL) functions, and the Memory and Cable parity status/control. Programming the SIO/2, CTC, DMA Controller and the Character/Master monitor is the responsibility of the system software and is acomplished primarily by execution of IN and OUT (I/O) instructions.

2.1 The TCB-1 memory is both the control store and data store for the CPU. The CPU control store is loaded by the 928 Data Link and execution begins at address X'0000' after a 928 Data Link RESTART command. If a Memory Parity Error (MPE) is detected during execution the CPU is forced to execute "NOP's", the Status Display is set with Light Emiting Diodes (LED's) SL1-SL7 "ON" and SL8 blinking (see 17.0), and the 928 Data Link MPE status is set (see 2.1).

2.2 At Power-On time the TCB-1 enters diagnostic mode (see 15.0).

2.3 The TCB-1 interrupt scheme is standard for the Z80A family except for the Character/Master monitor and DMA Controller. The

Character/Master monitor does not require the "RETI" instruction execution at the end of the interrupt service routines and should only have a "RET" instruction. The DMA controller is not a Z80 family component, and instead uses Channel 2 and 3 of the CTC to signal interrupts.

2.4 The "Deadman" timer may use the Non-Maskable CPU interrupt and; if enabled, will interrupt any procedure or routine regardless of the interrupt mode or state of the maskable interrupt flag (see the Z80A-CPU Technical Manual).

2.5 Vectored interrupts (MODE 2) allow fast service and easy mapping of the service routines through the use of the "Vector" table. The maskable interrupt priority, from highest to lowest, for each device follows:

Vectored Interrupt Priorities

2.6	Highest	Character/Master Monitor		
2.7		SIO	Channel A	Receiver
				Transmitter
				External/Status
			Channel B	Receiver
				Transmitter
				External/Status
2.8		CTC	Channel 0	BAUD Rate Clock
			Channel 1	Timer
			Channel 2	DMA Controller 0/2 EOP
	Lowest		Channel 3	DMA Controller 1/3 EOP

2.9 The CPU controls the TCB-1 through the I/O functions, an I/O address summary follows:

CPU Input/Output Address Space

	Address	Device	Channel	Function	
2.10	X'00'	SIO	Channel A	Data Registers	
	X'01'		Channel B	Data Registers	
	X'02'		Channel A	Control Registers	
	X'03'		Channel B	Control Registers	
2.11	X'07'	Status/Address		Switches, input only	
2.12	X'10'	DMA	Channel 0	SIO Channel A	Current Address
	X'11'				Cur't Word Count
	X'12		Channel 1	SIO Channel B	Current Address
	X'13'				Cur't Word Count
	X'14'		Channel 2	SIO Channel A	Current Address
	X'15'				Cur't Word Count
	X'16'		Channel 3	SIO Channel B	Current Address
	X'17'				Cur't Word Count
2.13	X'18'		CONTROL	Write Command/Read Status Reg.	
	X'19'			Write Request Register	
	X'1A'			Write Single Mask Register Bit	
	X'1B'			Write Mode Register	
	X'1C'			Clear Byte Pointer Flip/Flop	
	X'1D'			Write Master Clear/Read Temp.	
	X'1F'			Write All Mask Register Bits	
2.14	X'20'	CTC	Channel 0	BAUD Rate Clock, IxC	
	X'21'		Channel 1	Timer	
	X'22'		Channel 2	DMA Controller, EOP Ch. 0/2	
	X'23'		Channel 3	DMA Controller, EOP Ch. 1/3	
2.15	X'30'	DMA	Write Next Receiver Ch. on DMA Cont. 0/2		
	X'31'		Write Next Transmitter Ch. on DMA Cont. 1/3		
2.16	X'32'		Update Curr. Receiver Ch. on DMA Cont. 0/2		
	X'33'		Update Current Transmitter Ch. on DMA 1/3		
2.17	X'34'	Monitor	Base Register, Monitor Block/Char. Table		
	X'35'		Control Register/"Deadman" timer Control		
2.18	X'36'	Deadman	Resets "Deadman" timer (out only, no data)		
2.19	X'37'	ACU	Autocall unit Control/Status register		
2.20	X'40	Line Interface & Status Switches	Write Line Controls/Read Address/Status Switches		
2.21	X'50'	Diagnostics	Exit Diagnostic Mode		
	X'51'	OUT only,	Enable Memory Parity Generator		
	X'53'	no data	Disable Memory Parity Generator		
2.22	X'60'	928 Type	Read 928 Device Type		
2.23	X'70'	Status Display	Write TCB-1 Status Display		

2.24 I/O addresses not explicitly described above should not be selected, since device addresses are only partially decoded and device confusion will result.

SIO/2 Functions

3.Ø The SIO/2 element, operating on a 4MHz (25Ø.4ns) clock, converts data from 8 bit parallel format to one of several serial formats and vice versa. In addition, the SIO/2 performs character and line buffering; line control and status monitoring; and error protection and detection. Both Synchronous and Asynchronous line displines are supported. Synchronous mode supports both Bit Oriented Protocols (BOP's) and Character Oriented Protocols (COP's). Asynchronous mode (Start/Stop) allows variable data, stop bit, and parity fields. The Z8ØA-SIO Technical Manual contains a complete description of the various modes and line disciplines.

3.1 The CPU controls the SIO/2 functions by I/O instructions as outlined in 2.1Ø. The CPU may also select data line encoding, NRZ to NRZI conversion, and internal or external BAUD rate clock by OUTPUT to the Line Control Register (see 13.Ø).

3.2 Within the SIO/2, Channel A is configured as the Receiver and Channel B as the Transmitter; this configuration allows fullduplex DMA operations by using the WAIT/READY function of each channel. Channel A DMA request (W/RDYA) may be routed to either Channel Ø or Channel 2 of the DMA Controller. Equivalently, Channel B (W/RDYB) may be routed to either Channel 1 or Channel 3 of the DMA Controller (see 4.2). Two SIO/2 inputs, DCDB and CTSA, are used to monitor MODEM signals Data Set Ready (DSR) and Ring Indicator (RI), respectively. Channel A's Transmitter is looped back into Channel B's receiver for diagnostic use.

3.3 SIO/2 Controls

Control	Type	Function
TxCA	Input	Internal Clock (IxC) derived from CTC Ch. 1
RxCA	Input	Reciver Clock, selectable Internal/External
DCDA	Input	Carrier Detect from MODEM (DCD)
RxDA	Input	Received Data from MODEM
RTSA	Output	not used
CTSA	Input	Ring Indicator (RI)
TxDA	Output	looped back to RxDB
TxCB	Input	Transmitter Clock, selectable Int/Ext
RxCB	Input	Internal Clock (IxC)
DCDB	Input	MODEM Data Set Ready (DSR)
RxDB	Input	looped back from TxDA
RTSB	Output	Request To Send (RTS),
CTSB	Input	Clear To Send (CTS)
TxDB	Output	Data Transmited to MODEM
W/RDYA	Output	request DMA Controller Channel Ø/2 service
W/RDYB	Output	request DMA Controller Channel 1/3 service
RESET	Input	Processor RESET or Memory Parity Error

9517A-DMA Controller

4.Ø The DMA Controller, operating on a 5ØØ.8ns clock, allows high speed data transfer between the SIO/2 and TCB-1 memory. The CPU controls the function of the DMA Controller through I/O instruct- ions as outlined in 2.12, 2.15, and 2.16.

4.1 The SIO/2 Receiver (Channel A) and Transmitter (Channel B) are double buffered by the DMA controller and the associated circuits. Channels Ø and 2 support data input for the SIO/2 Receiver and are called the Receiver Channel pair, likewise, Channels 1 and 3 support data output for the SIO/2 Transmitter and are called the Transmitter Channel pair.

4.2 The Next and Current Channel Registers, one set for each DMA Channel pair, control the routing of the SIO/2 DMA requests to one of the channels in the pair (these are external registers not inside the DMA Controller). When an End Of Process (EOP) is signaled by the DMA Controller for a particular channel pair, the Next Channel Register is copied into the Current Channel Register effectivly switching to the next desired channel; in addition the CTC will signal an interrupt for that pair.

4.3 This type of channel switching allows the system sofware to set the Next Channel Register to the inactive channel of that pair, program all the required register values for the next desired memory buffer, and then unmask the channel to await EOP on the active channel. When the EOP occurs, the "Next" is copied to the "Current" register, W/RDYx is routed to the previously inactive channel and future requests are honored by the newly selected channel.

4.4 The DMA Controller options must be set for Extended Write, DACK outputs active LOW, DREQ inputs active high, single byte transfer mode, and rotating DREQ priority.

4.5 CTC Channels 2 and 3, Clock/Trigger inputs, monitor the DMA Channel pairs Ø/2 and 1/3, respectively, for an EOP. The CTC should request an interrupt if either of the inputs go low (=Ø) and provide the "Vector" during Interrupt Acknowledge (see 5.Ø).

CTC Functions

5.Ø The CTC provides the TCB-1 with timing and counting functions. Channel Ø, with a Clock/Trigger input of 2MHz (5ØØns), is used to generate an Internal Clock (IxC) which may be routed to the SIO/2 Receiver and/or Transmitter. Channel 1 is used for software event timing. Channel 1's Clock/Trigger input is IxC generated by Channel Ø; this allows Channels Ø and 1 to operate in a cascaded mode. Channels 2 and 3 are used to alert the CPU of DMA completion (see 4.5).

5.1 The CTC is programmed by the CPU and is mapped in the I/O space as outlined in 2.14. Channel Ø may programmed for either counter mode or timer mode depending on the desired BAUD rate. The ZC/TOØ output (Channel Ø) rate is divided by two to produce a 5Ø/5Ø duty cycle Internal Clock (IxC). This clock is supplied to the SIO/2, the RS-232-C interface (pin 11), CTC Channel 1, and to the Internal/External Clock selector (see 13.Ø). The RS-449 interface may selectively emit, on the TT signal, either the external clock (ST) or the Internal Clock (IxC) (see 13.Ø). Channel 1 may be programmed for either timer mode or counter mode

operation to generate an interrupt on each time-out. Timer mode allows a number of system clock cycles (16*N, or 256*N, where 1<=N<=256) to expire before generating each interrupt, while Counter mode counts a number (1<=N<=256) of IxC clock cycles before generating each interrupt. Channels 2 and 3 monitor the DMA Controller's EOP signal for each Channel pair and should both be programmed for count mode operation to interrupt on a single falling edge of the Clock/Trigger input.

Deadman Timer

6.0 The "Deadman" timer prevents the communications line from being "jammed" by the TCB-1 in the event of a software/hardware failure. The CPU controls the "Deadman" timer functions through I/O instructions as outlined in 2.17 and 2.18. Two control bits, DNMI and DDMT, are provided to select the timer options and are concatenated with the Monitor Control bits (see 9.2). The timer must be used whenever Request To Send (RTS) is to be presented to the MODEM. It may also be used as a general software time-out device to produce a Non-Maskable Interrupt. Once enabled, the timer should be periodically reset by the system software at least every Ø.5 seconds to prevent its expiration (approx. Ø.7 seconds).

6.1 If DNMI is set to one, the CPU will not be interrupted regardless of the state of the "Deadman" timer. If DNMI is set to zero, the CPU will be unconditionally interrupted when the timer expires, via Non-Maskable Interrupt (NMI) to X'ØØ66'. The DNMI bit should only be set to one, disabling the NMI, before the DDMT (see 6.2) is set (=1) to disable the timer. It should only be reset (=Ø) after the DDMT is reset (=Ø), to enable the timer (i.e. the DNMI state change should always be bracked by the state change in DDMT). If the "Deadman" interrupt is enabled, Vector memory will be mapped out of the Processor memory space when the interrupt (NMI) is active (timer has expired), regardless of the state of MAPOUT. This prevents NMI instructions (at X'ØØ66') from being fetched from Vector Memory mapped in at X'ØØØØ'.

6.2 DDMT enables the "Deadman" timer. Setting DDMT to one will stop the timer function and disable the RTS signal to the MODEM. If the NMI function is being used it must be turned off before the timer is disabled. Setting DDMT to zero will start the timer and allow a RTS signal to be presented to the MODEM. If the NMI function is desired, it must be enabled (=Ø) after the DDMT bit is reset (=Ø).

Character and Master Monitors

7.Ø The Character and Master monitors provide supervisory services for the TCB-1. Each monitor alerts the CPU if a specific memory write occurs. The Character monitor "watches" characters deposited by the DMA controller, while the Master monitor "watches" the 928 Data Link memory write accesses. Each monitor may "watch" for several different events, simultaneously (up to 1Ø24).

7.1 The Character monitor allows the TCB-1 to process Binary Synchronous Communication (BSC) protocols with a minimum of system overhead; but its uses are not limited to the BSC class. The Character monitor can interrupt the CPU when any specific characters (control, format, etc.) are deposited in memory. Thus, the CPU can perform an immediate action such as disabling the Receiver CRC, switch DMA buffers, etc..

7.2 The Master monitor can interrupt the CPU when specific memory addresses are write accessed by the "Master". This "Master" interrupt can be used to queue another request, awaken a sleeping task, etc.. The monitors share the Control register, the Base register, the First In First Out memory (FIFO), and the 1Ø24 byte Vector memory.

Monitor FIFO

8.Ø The Monitor First In First Out memory (FIFO) may hold up to sixteen vectors awaiting CPU acknowledgement. Either monitor may deposit vectors in the FIFO. In the event of a FIFO overflow,

either a X'ØØ' or X'8Ø' vector will be deposited in the FIFO to indicate which monitor was the last to overflow (this does not mean that only one monitor overflowed but that it was the last one to overflow). Therefore, Vectors X'ØØ' and X'8Ø' are reserved and should not be used by other devices. As Vectors are deposited in the FIFO the LSB, VØ, will be reset to zero and the MSB, V7, will be set to reflect which monitor acted in the deposition. VØ = Ø assures that all Interrupt Service Routine Program Counters are aligned on a halfword boundaries. V7 = 1 indicates a Character monitor vector, while V7 = Ø indicates a Master monitor vector.

Monitor Control Register

9.Ø The Monitor Control register contains eight control bits, six of which determine the mode of monitor operation. The two remaining bits control the "Deadman" timer. The CPU controls the contents of the Monitor Control register which is mapped in the I/O space as outlined in 2.17. The contents of the Monitor Control register are all set (=1) at Processor RESET time. The Control bits have the following configuration:

Monitor Control Register Format

9.1

Data Bit Position	Control Bit Name	Function
DØ	MAPOUT	Removes Vector memory from Processor memory space
D1	CHARMON	Enables Character monitor function
D2	MASMON	Enables Master monitor function
D3	CLRINT	Clears all pending interrupts
D4	INTALL	Forces VØ = Ø, generates interrupt on all characters
D5	BUFOFF	Disables buffering by SIO-DMA pair
D6	DNMI	Disables "Deadman" NMInterrupt
D7	DDMT	Disables "Deadman" timer

9.2

MAPOUT

9.3 The Vector memory may be selectively mapped into the Pro-

cessor memory space by this bit. When set to zero, the Vector memory appears at the address contained in the Monitor Base register (upper six bits only). When set to one, the Vector memory is removed from the Processor memory space. The state of MAPOUT may be changed at any time, regardless of other Monitor Control bit states.

CHARMON

9.4 The Character monitor may be selectively enabled or disabled by this bit. When set to one, the characters deposited by the DMA controller are "Looked-Up" in the Vector memory to see if a CPU interrupt is required. The bit state may be changed at any time and does not affect vectors previously stored in the monitor FIFO.

MASMON

9.5 The Master monitor may be selectively enabled or disabled by this bit. The Master monitor is active when this bit is set to one. The bit state should only be changed when the 928 Data Link is polling or inactive (i.e. not while 928 Data Link may be writting in the monitor block). Changing the bit's state has no effect on vectors previously stored in the monitor FIFO.

CLRINT

9.6 The monitor FIFO may be purged by this control bit. After the CPU interrupts are disabled, this bit may be set to one to discard all pending interrupts and allowed no other interrupts until the bit is reset. CLRINT may be reset (=Ø) any time except when the MASMON bit is enabled (=1), in this case it may be reset when the 928 Data Link is polling or inactive (i.e. not writing in the monitor block).

INTALL

9.7 When set to one, this bit forces VØ to zero when a character is "Looked-Up" in Vector memory. Therefore all characters generate interrupts regardless of the value of VØ in Vector memory. INTALL allows easy handling of paired control characters. The state of this bit may be changed at any time, regardless of the state of any other monitor control bits.

BUFOFF

9.8 This bit is used to control DMA controller write access (Channels Ø and 2) to TCB-1 memory. If this bit is set (=1), no restrictions are placed on the DMA controller memory access and transfers are made as soon as the character is loaded in the SIO/2 Receiver FIFO. If this bit is reset to zero, the DMA controller write access is prohibited when a Character Vector is loaded in the monitor FIFO. After the vector is acknowledged, the access is restored by the first DMA controller I/O access (by the CPU) in the Character Interrupt Service routine. Therefore, the DMA controller must wait for the Character Vector to be passed to the CPU (entry to the service routine) and then for the CPU to access any DMA control register. This will allow information to be retrieved from, or provided to, the DMA controller concerning either the character that was just deposited or the next character in the SIO/2 Receiver. Only one CPU I/O access is allowed before the DMA controller memory access is restored. If the information transfer requires more than one I/O access, the channel request, DREQx, should be masked to prevent a waiting request from being serviced and disturbing the state of the channel registers.

Monitor Base Register

10.Ø The Monitor Base register contains the 1K block address for Vector memory. It also indicates the area in TCB-1 memory which

is used for communications with the "Master", hereafter called the Monitor block. Only the six most significant bits are used in the block address recognition process. The remaining two bits are used in the Character monitor to select the recognition table. The CPU controls the contents of the Monitor Base register which is mapped in the I/O space as outlined in 2.17.

10.1 Note: The Monitor Base address (upper six bits, MBA10-15) should not be changed while the Master monitor is enabled, although the lower two bits (MBA8 and MBA9) may be changed any time.

Vector Memory

11.0 The Vector Memory contains information to determine which memory events should generate interrupts and the vectors that are passed to the CPU to indicate which events occured. The memory is shared between the Character and Master monitor. It consist of two 4 X 1024 bit static memories (2114-A's) arranged as 1024 eight bit bytes. The Vector Memory bits are referred to as V0-V7, with V0 being least significant.

11.1 V0 = 0 activates a location as a potential Character Vector, and V7 = 0 does likewise for a Master Vector. V7 is set to indicate which process caused the vector to be deposited in the FIFO (Character = 1 and Master = 0). The remaining bits, V1-V6, are passed on as they were programmed in Vector Memory. With the above constraints, a single Vector Memory location may be shared between the two monitors.

11.2 The Vector Memory may be mapped into the Processor memory space at the address loaded in the Monitor Base Address register (see 10.0). Access to the Vector Memory has no effect on TCB-1 memory normally found at the same address. Vector memory is transparent to the 928 Data Link and does not affect its TCB-1 memory access. When the Vector memory is mapped into the memory space, the CPU may perform any type of memory access (such as Read cycles, Write cycles, even M1 Instruction Fetch cycles; although M1 cycles are not reccommended and care should be used when mapping in Vector Memory not to attempt to access TCB-1

memory normally found at the Vector memory address).

11.3 The Vector Memory has the lowest access priority. For example, if the Vector Memory were mapped in at the same location as Diagnostic PROM (X'FØØØ'-X'FFFF' when in Diagnostic Mode) the Memory Read Cycle would select PROM, while the Memory Write cycle would select Vector Memory. If the "Deadman" timer interrupt is enabled (DNMI), Vector Memory access will be inhibited if the timer has expired; this prevents instructions from incorrectly being fetched from Vector Memory (in the event that Vector memory is mapped into the Processor space at X'ØØØØ'-X'Ø3FF').

11.4 The Vector Memory is interrogated for each memory cycle. If a DMA Controller Write cycle is active, the Vector Memory address is created from the data word (character) being stored(i.e. a direct memory lookup). Since a character is only eight bits, the remaining two bits (1Ø bits in all) are taken from the least significant positions of the Monitor Base register, thus allowing one of four different tables, of 256 bytes each, to be used in the lookup process (MBA8 and MBA9 are table select bits).

11.5 The character lookup address mapping is:

D0 = VA0, D1 = VA1, D2 = VA2, D3 = VA3, D4 = VA4,D5 = VA5, D6 = VA6, D7 = VA7, MBA8 = VA8, and MBA9 = VA9

Where DØ-D7 is the character value, MBA8 and MBA9 are table select bits, and VAØ-VA9 is the Vector Memory address value obtained.

11.6 VØ of the vector obtained from the above address is checked and if zero the vector is placed in the monitor FIFO. The FIFO will then request an interrupt of the CPU. Alternately, the VØ bit may be forced to zero by setting INTALL, a control bit in the monitor control register, which causes all characters to generate an interrupt (useful in paired control character cases, e.g. DLE SYN).

11.7 The Master monitor operates on a selected area of TCB-1 memory. Any one kilo-byte (1K) memory block, which resides on a 1K address boundary, may be "watched". The memory block, hereafter called the Monitor Block, is specified in the Monitor Base

register. The Vector memory has a one to one address correspondence to this block. During a 928 Data Link Write access, if V7 of the Vector obtained from Vector memory is zero the Vector is deposited in the monitor FIFO. The FIFO will present an interrupt request and pass the vector to the CPU during Interrupt Acknowledge. Any number of bytes in the 1K block may be "watched". In some systems, monitoring the semaphore bytes, which indicate that a service has completed and that another may be started, would be ideal use of the Master monitor. In this case, a "Pipe Line" operation could be established to provide fast "Master" services.

Automatic Calling Unit (ACU)

12.Ø The RS-366 ACU Interface allows the TCB-1 to orignate dialed calls. The CPU controls this interface through the I/O instructions as outlined in 2.19. The MODEM signals RI or IC, and TM; and the Memory Parity Error register (MPE) are appended to the status register. The SF/RF MODEM signal (see RS-449) is appended to the control register. The format of the Control/Status register follows:

ACU Register Format

12.1

Data Bit	Ø	1	2	3	4	5	6	7
Control	NB1	NB2	NB4	NB8	DPR	CRQ	zero	SF/RF
Status	ACR	PND	PWI	COS	DLO	RI	TM	MPE

Note: All bits are positive logic; ON=1; OFF=Ø.

Line Interface

13.Ø The Line Interface register allows the TCB-1 to select Internal or External SIO/2 Receiver clock, Internal or External SIO/2 Transmitter clock (the RS-449 signal TT is identical to the SIO/2 Transmitter clock), NRZI or NRZ line encoding, and RS-449 or RS-232C interface. The CPU controls the Line Interface Reg-

ister through I/O instructions as outlined in 2.20. Only Data Bits 0-3 are used, the others should be set to zero.

Line Control Register Format

13.1

Data Bit	0	1	2	3
Control Select	Rx INT/EXT 1 = EXT	Tx INT/EXT 1 = EXT	NRZI/NRZ 1 = NRZ	RS-449/232C 1 = 232C

Address/Status Switches

14.0 The Address/Status switches enable the TCB-1 to obtain configuration information. The eight switch settings could be an address within a network or a status indicating an expected TCB-1 operation. Therefore, the switch settings are software specified. The switch settings are obtained by a CPU IN instruction and is mapped, twice for software compatibility, in the I/O space as outlined in 2.11 and 2.20. The ON position is Binary 1, Switch 1 is Data Bit 0, Switch 2 is Data Bit 1, etc..

Diagnostic Functions

15.0 The TCB-1 provides several diagnostic functions. The Memory Parity Generator may be controlled by the CPU through OUT instructions as outlined in 2.21. If the Memory Parity Generator is disabled:

15.1
1) Fixed Parity is written to memory (Parity Bit=1) for all subsequent memory write accesses.
2) The status of the MPE register is inhibited in the 928 Data Link Status register.
3) The SIO/2 is not RESET on MPE error detection.
4) The CPU is not forced to execute "NOP's" on MPE error detection.

15.2 Memory Parity Error (MPE) may be examined by a CPU Input instruction from the ACU Status register (see 12.0). MPE may be cleared (MPE = 0) by setting or resetting the Memory Parity mode.

15.3 At Power-On time, the Processor section is RESET and the 928 Data Link transmitter is disabled (although the 928 Data Link

receiver remains functional). The CPU begins execution of forced "NOP's" at X'0000' (see 15.3) until it reaches instruction address X'F000', which triggers the TCB-1 into Diagnostic Mode and 4K bytes of EPROM (2716) is mapped into the memory space at address X'F000'. In the Diagnostic mode "forced" Memory Parity Error "NOP's" are inhibited.

15.4 If the diagnostics are completed the Status Display should be set to indicate the TCB-1 Status and the CPU should Exit Diagnostic Mode by an Output instruction (see 2.21). The EPROM will be mapped out of the memory space, and the 928 Data Link transmitter enabled. "NOP's" will be executed until the 928 Data Link deposits the control store and signals RESET. Otherwise, the Diagnostic status should be set and the CPU "HALT'ed".

15.5 The "Master" may terminate the TCB-1 Diagnostic mode by sending RESTART to the 928 Data Link. This may cause problems in some systems if the Power-On Diagnostics are to be reexcuted, therefore it is recommended that the coaxial cables be disconnected in this case. The primary advantage in allowing the 928 Data Link to force an exit from Diagnostic mode during debugging, where the current program is to be purged by the RST button (on the front panel) and new code is to be loaded. Sometime after depressing the RST button, the "Master" will attempt to poll the TCB-1's SCA area; the 928 Data Link transmitter is disabled and the poll fails. The "Master", after several attempts belives the TCB-1 is "Dead", and will attempt to revive it by "Bootstraping" (IPL) ; the resulting RESTART command forces Diagnostic mode exit and normal program excution at X'0000'.

928 Device Type Switches

16.0 The 928 Device Type switch settings may be obtained by a CPU Input instruction. The I/O address is specified in 2.22. Data Bits 4-7 contain the switch value; Bit 4 is the LSB of the switch. The ON position is binary 0.

Status Display and Switches

17.Ø The Status Display register provides signaling to a front panel mounted Light Emitting Diode (LED) display, and allows a variety of condition to be displayed to the system operator. The Status Display is controlled by CPU OUT instructions as outlined in 2.23.

17.1 Seven of the LED's, Data Bits Ø-6 corresponding to SL1-SL7, are general purpose and may be assigned on the faceplate by a plastic overlay. The eighth LED, Data Bit 7, signals the functional state of the TCB-1: OFF indicates no power, ON blinking indicates diagnostic status, and ON continuous indicates normal status. The Status Display will be set with LED's SL1-SL7 "ON", and SL8 blinking any time the CPU is being forced to exe- cute "NOP's" (i.e. the Processor is not operating). This occurs at Power-ON, normal exit from Diagnostic mode, and during Memory Parity Error execution suspension.

17.2 The display panel also provides two momentary contact switches, "DIS" signals the communication interface to inactivate the Data Terminal Ready signal and "RST" generates a Power-On Reset state.

Status Display Bits

17.3

Data Bit	Ø	1	2	3	4	5	6	7
Display LED	SL1	SL2	SL3	SL4	SL5	SL6	SL7	SL8
Binary 1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Binary Ø	ON	ON	ON	ON	ON	ON	ON	Blinking

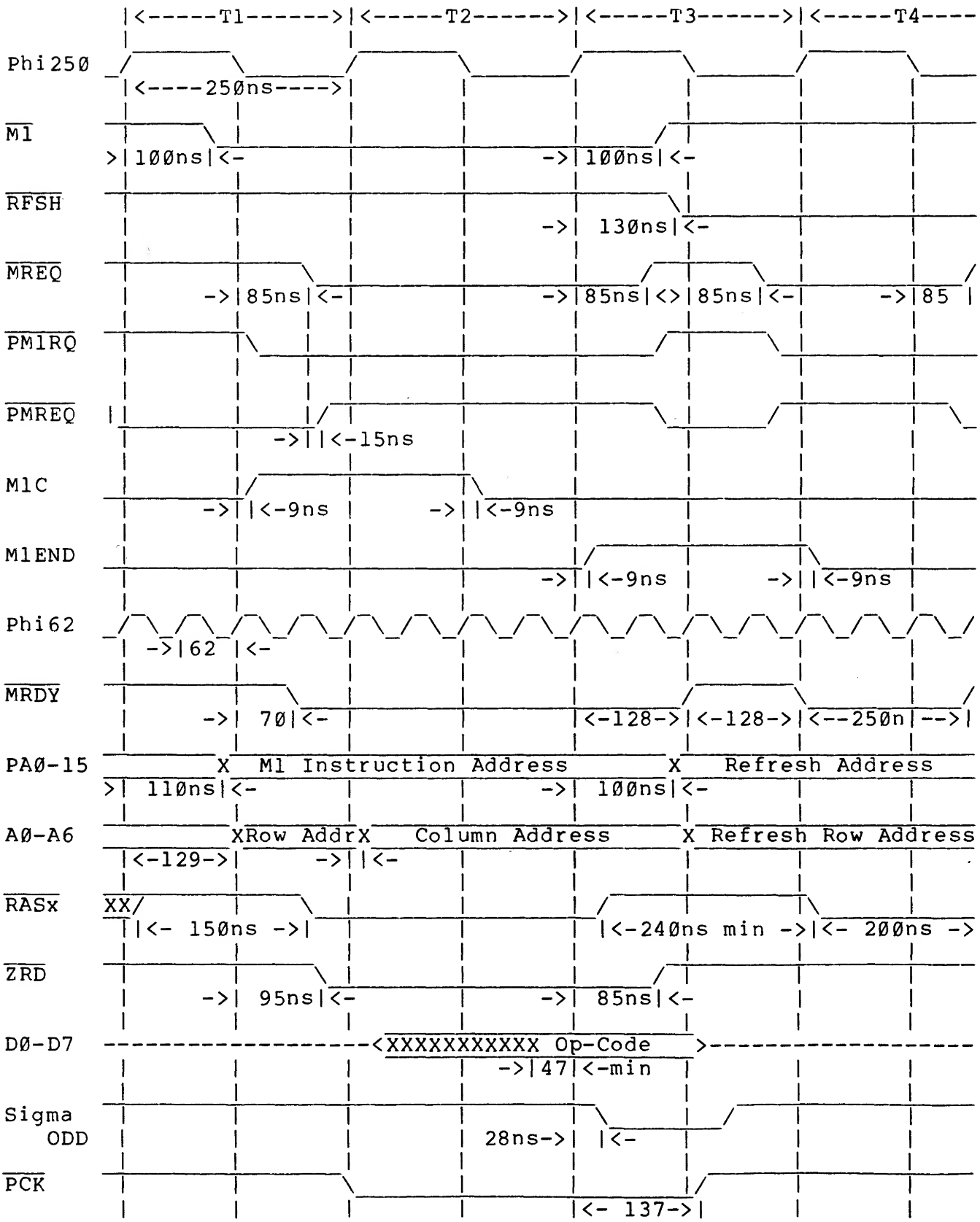
Telecommunication Processor

Timing Diagrams

The following diagrams indicates signal relationships for each section within the TCB-1. All signal names are capitol letters, Greek letters are spelled in English equivalents (i.e. Phi, Rho, Theta, Mu).

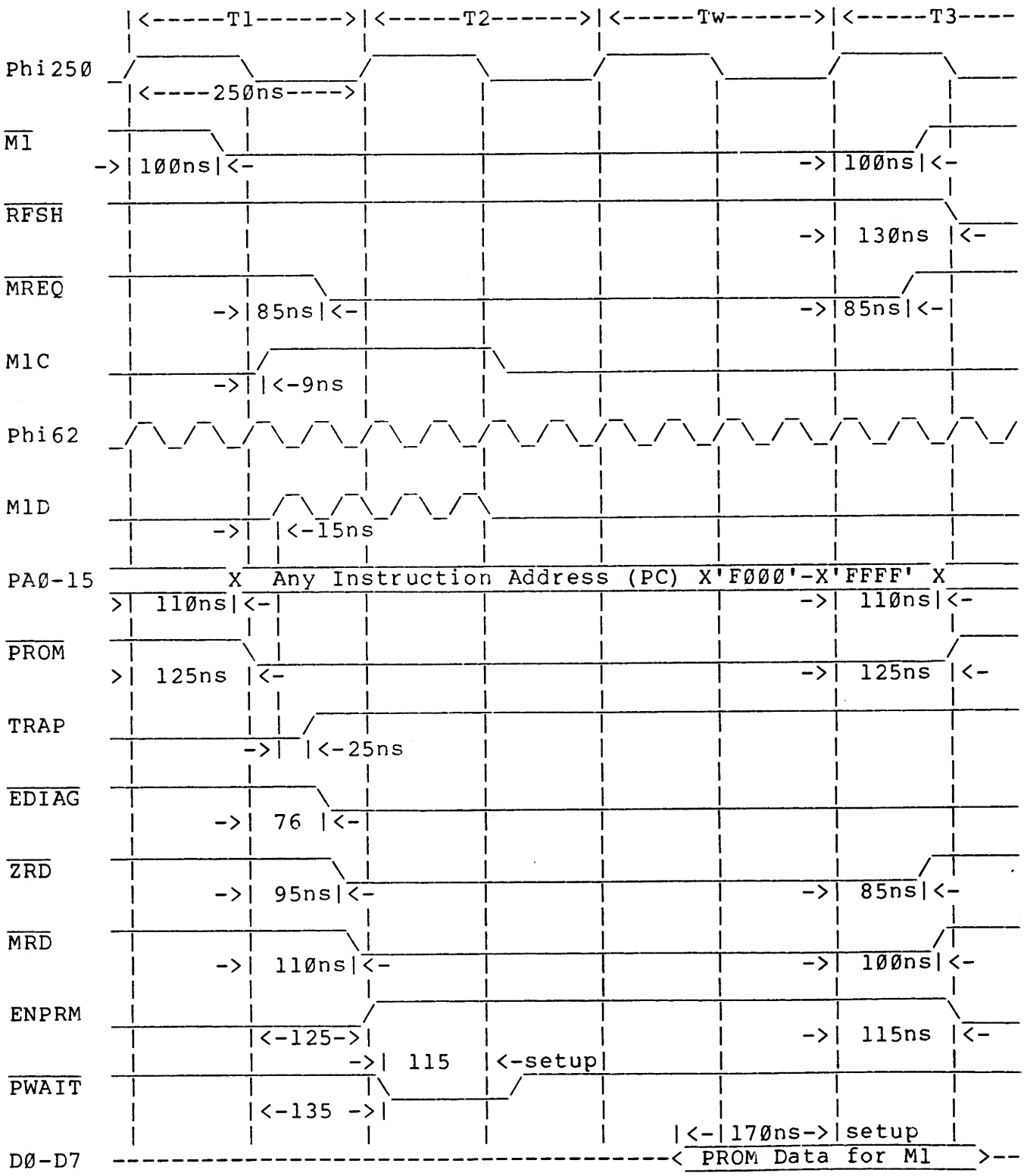
CPU M1 Cycle

Scale: 15.6ns/sp



CPU M1 Cycle from PROM

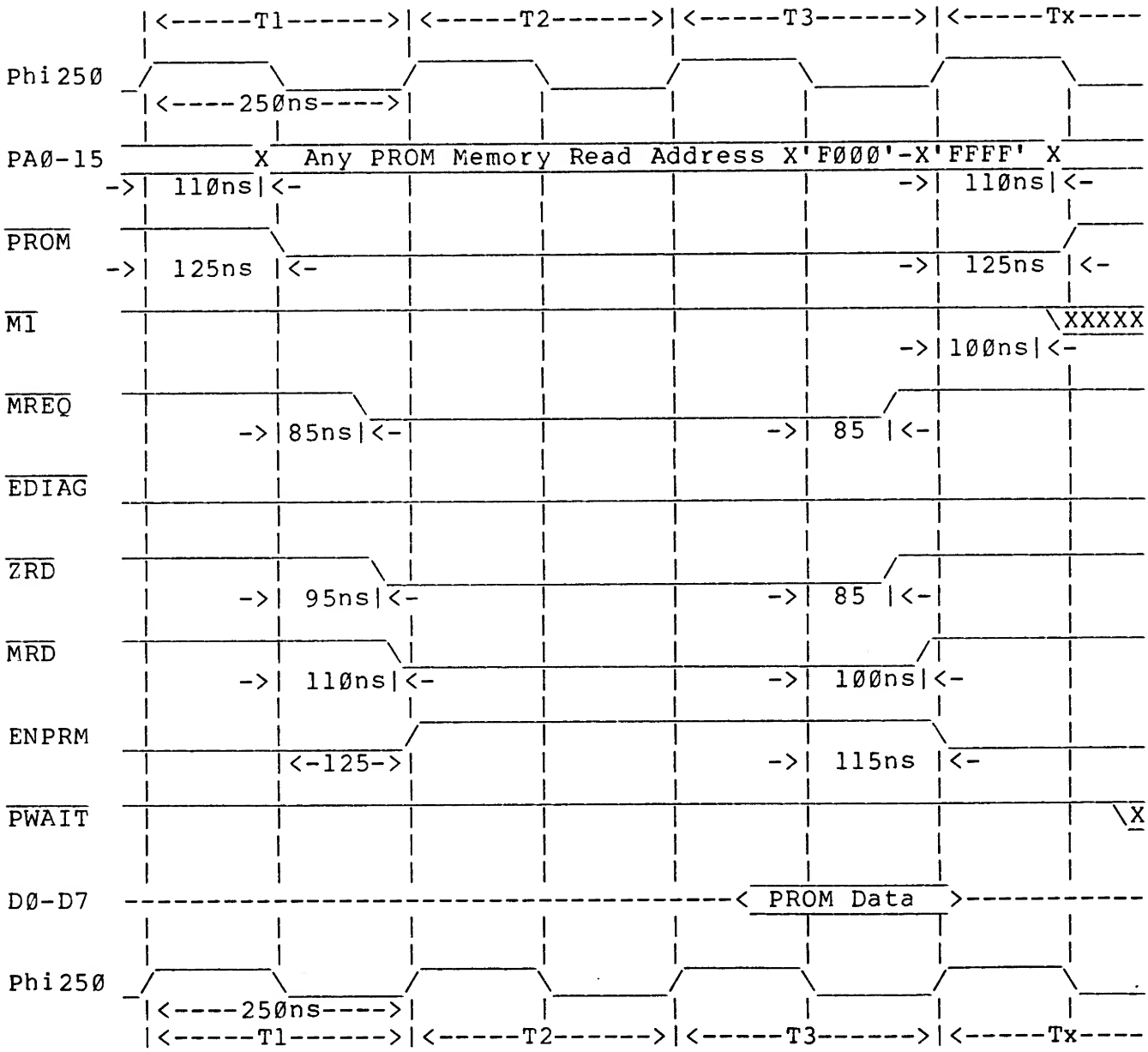
Scale: 15.62/ns



Note: $\overline{\text{RESET}}$, $\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, and $\overline{\text{WR}}$ are inactive (High).

CPU Read Cycle from PROM

Scale: 15.62/ns

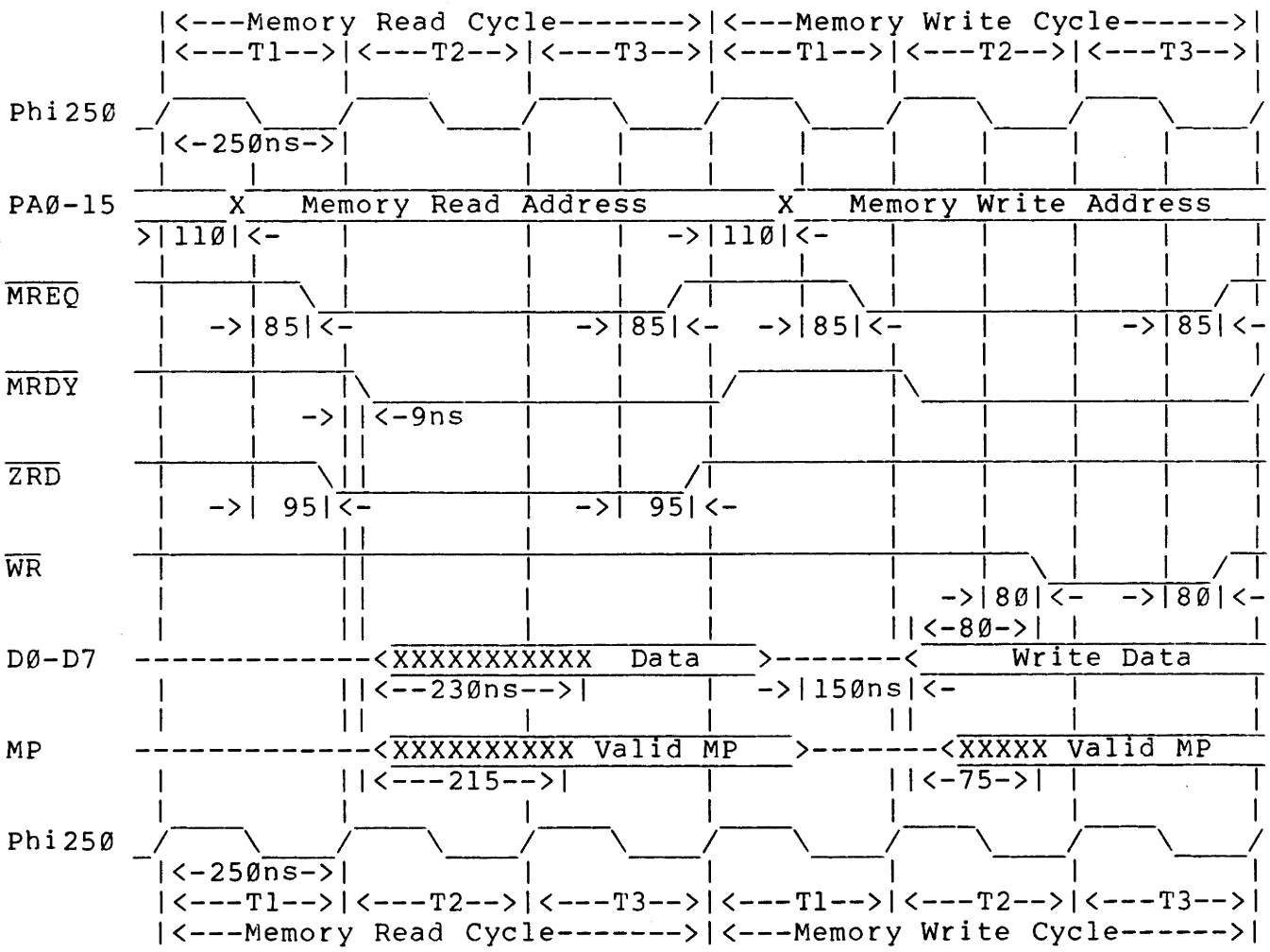


Note: RESET, BUSRQ, BUSAK INT, IORQ, M1, WR and RFSH are inactive.

CPU Memory Read and Write Cycle

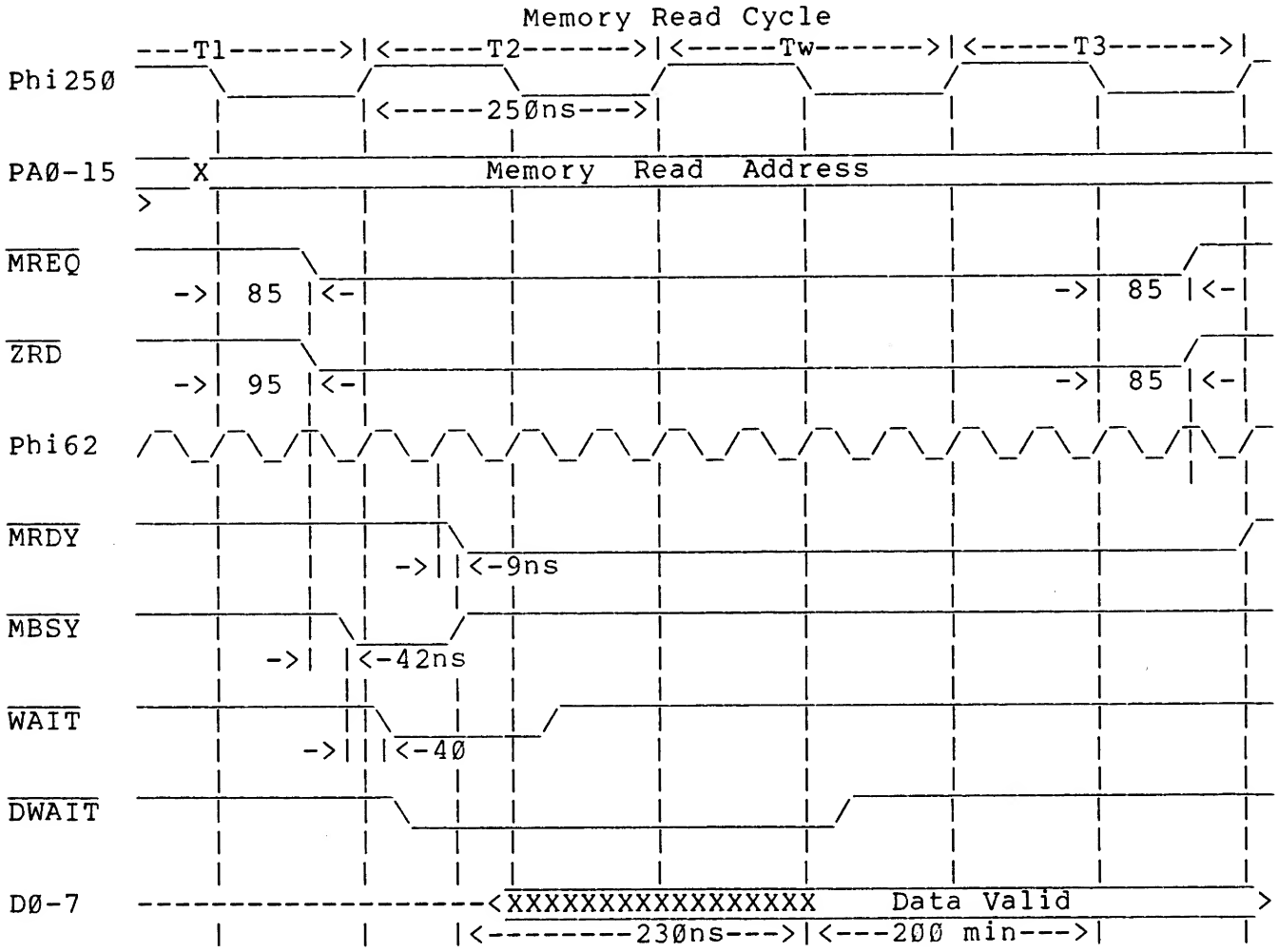
Scale: 25ns/sp

No memory contention.



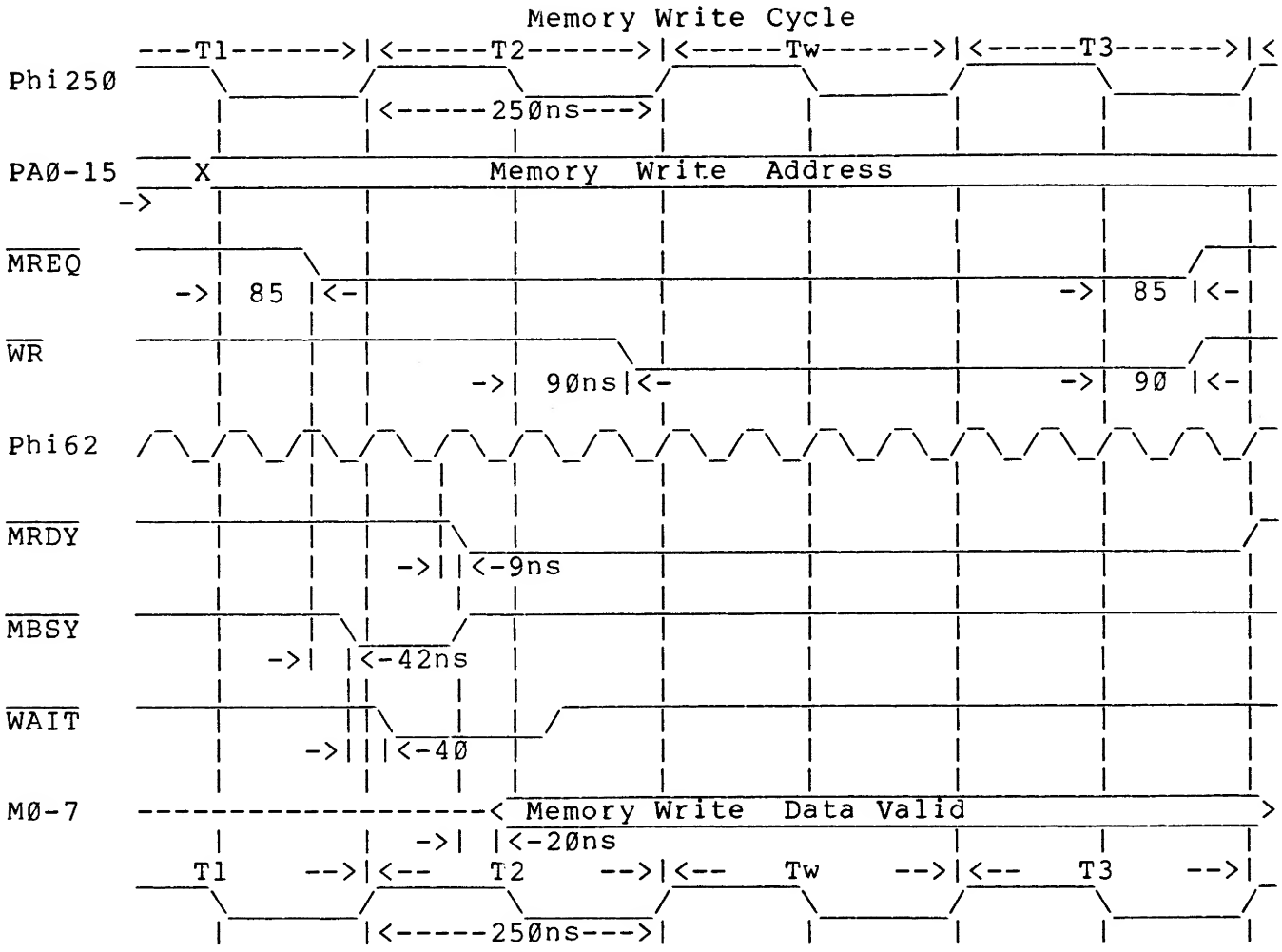
Note: $\overline{\text{RESET}}$,$\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ and $\overline{\text{RFSH}}$ are inactive (High).

CPU Memory Read Cycle
With Memory Contention
Scale: 15.6ns/sp



Note: $\overline{\text{RESET}}$,$\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, $\overline{\text{M1}}$, $\overline{\text{WR}}$ and $\overline{\text{RFSH}}$ are inactive.

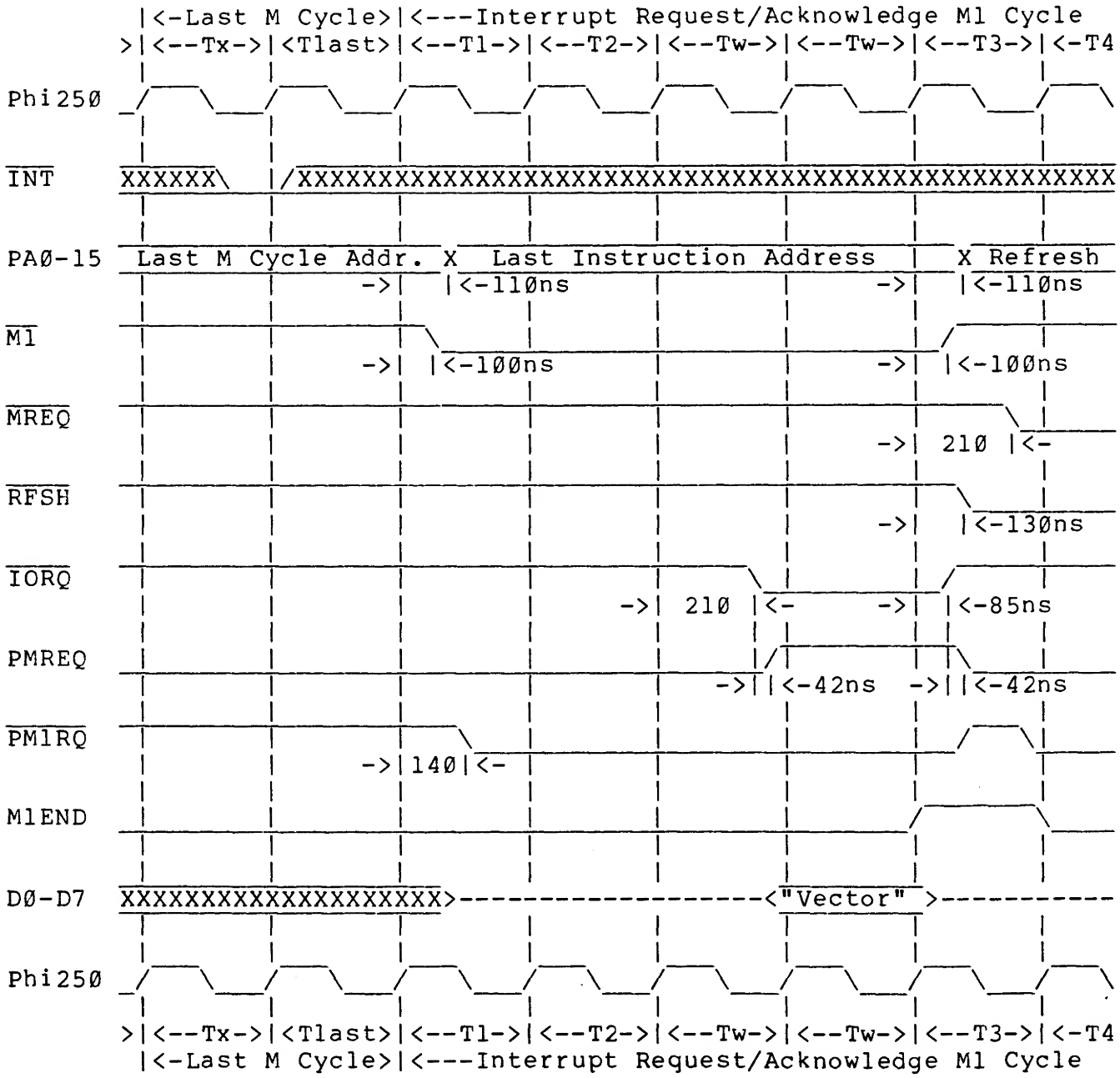
CPU Memory Write Cycle
With Memory Contention
Scale: 15.6ns/sp



Note: $\overline{\text{RESET}}$,$\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, $\overline{\text{M1}}$, $\overline{\text{RD}}$ and $\overline{\text{RFSH}}$ are inactive.

CPU Interrupt Request/Acknowledge Cycle

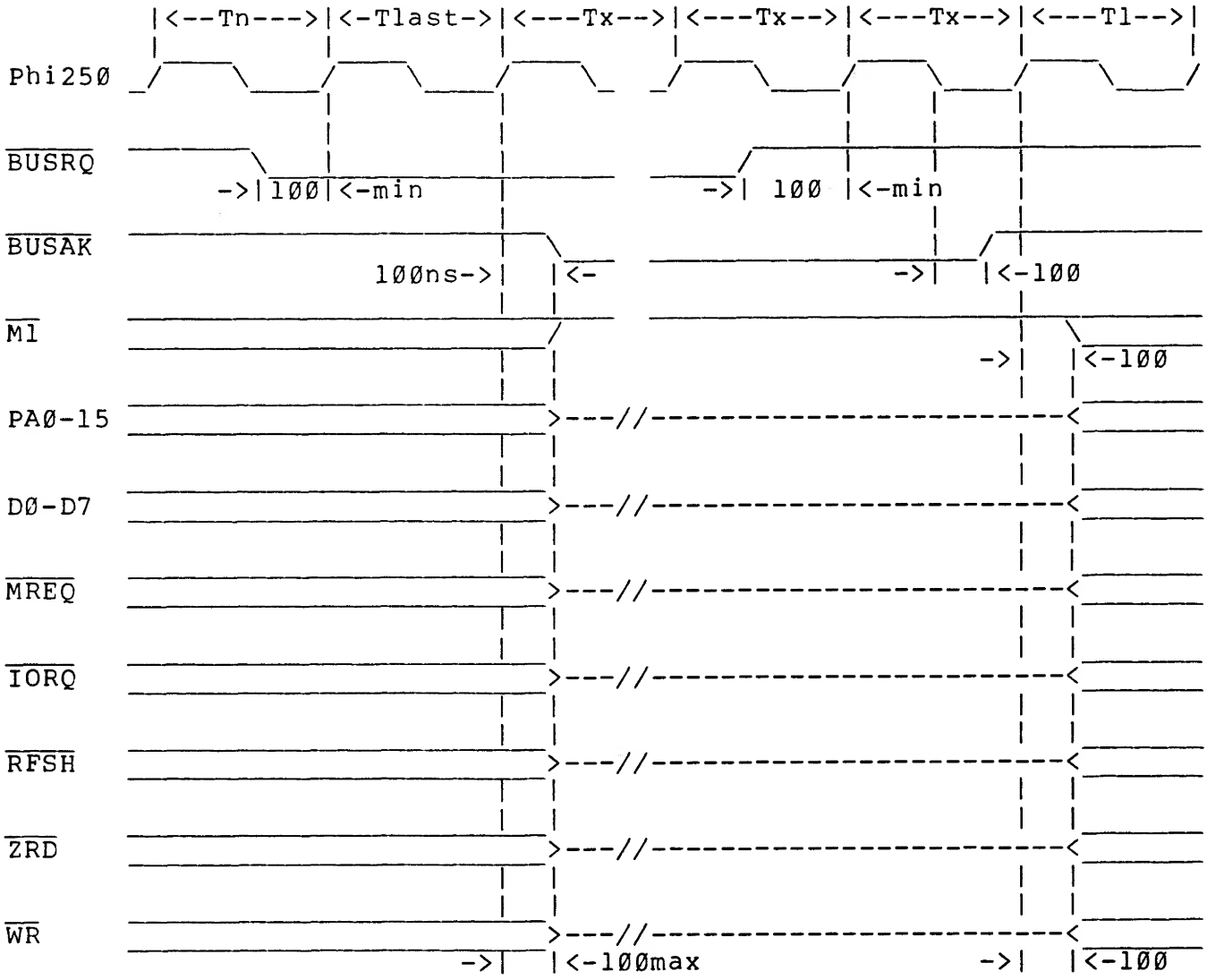
Scale 31.25ns/sp



Note: $\overline{\text{RESET}}$,$\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{ZRD}}$, and $\overline{\text{WR}}$ are inactive (High).

CPU Bus Request/Acknowledge Cycle

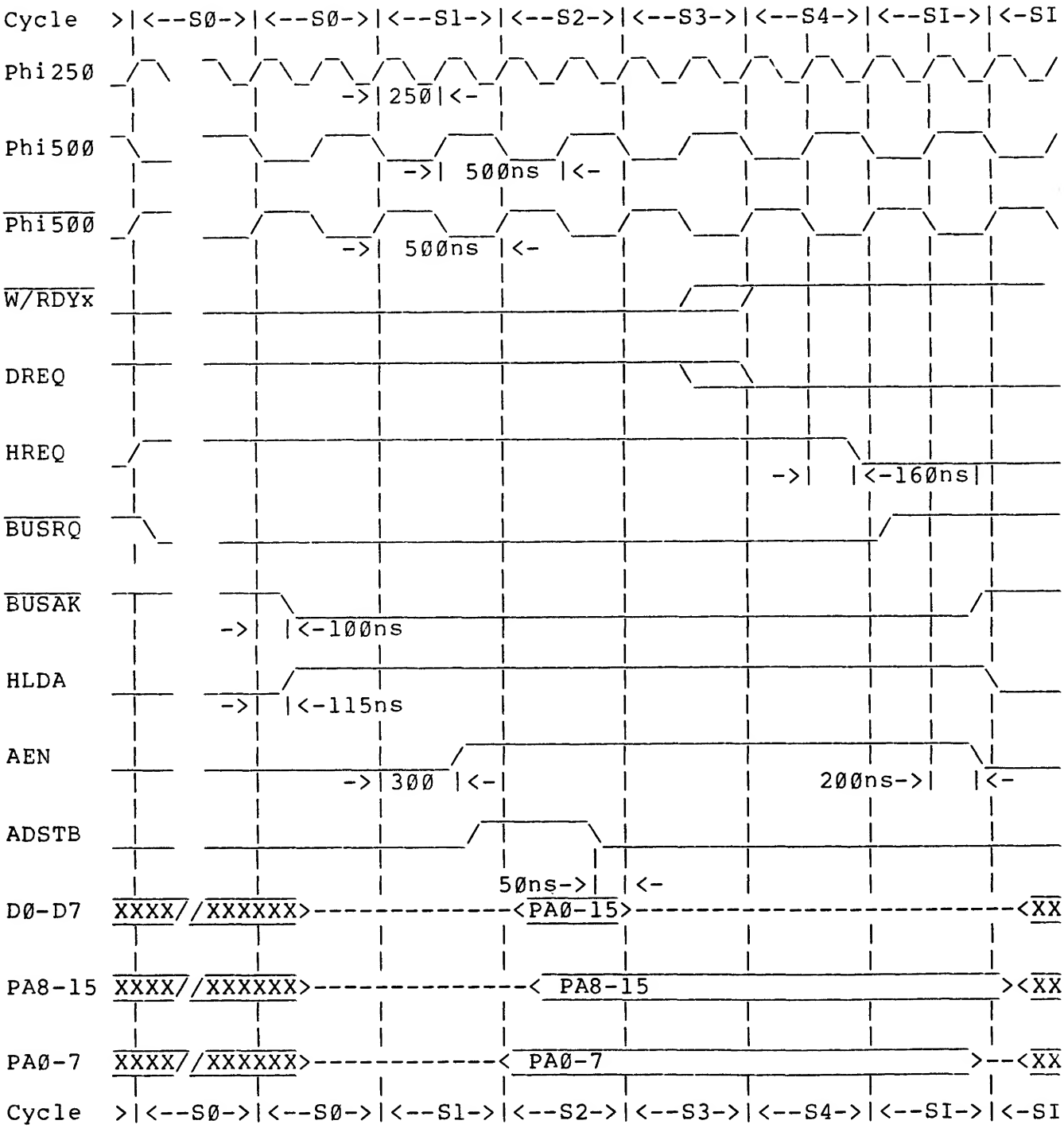
Scale: 25ns/sp



9517A-DMA Controller

Bus Control

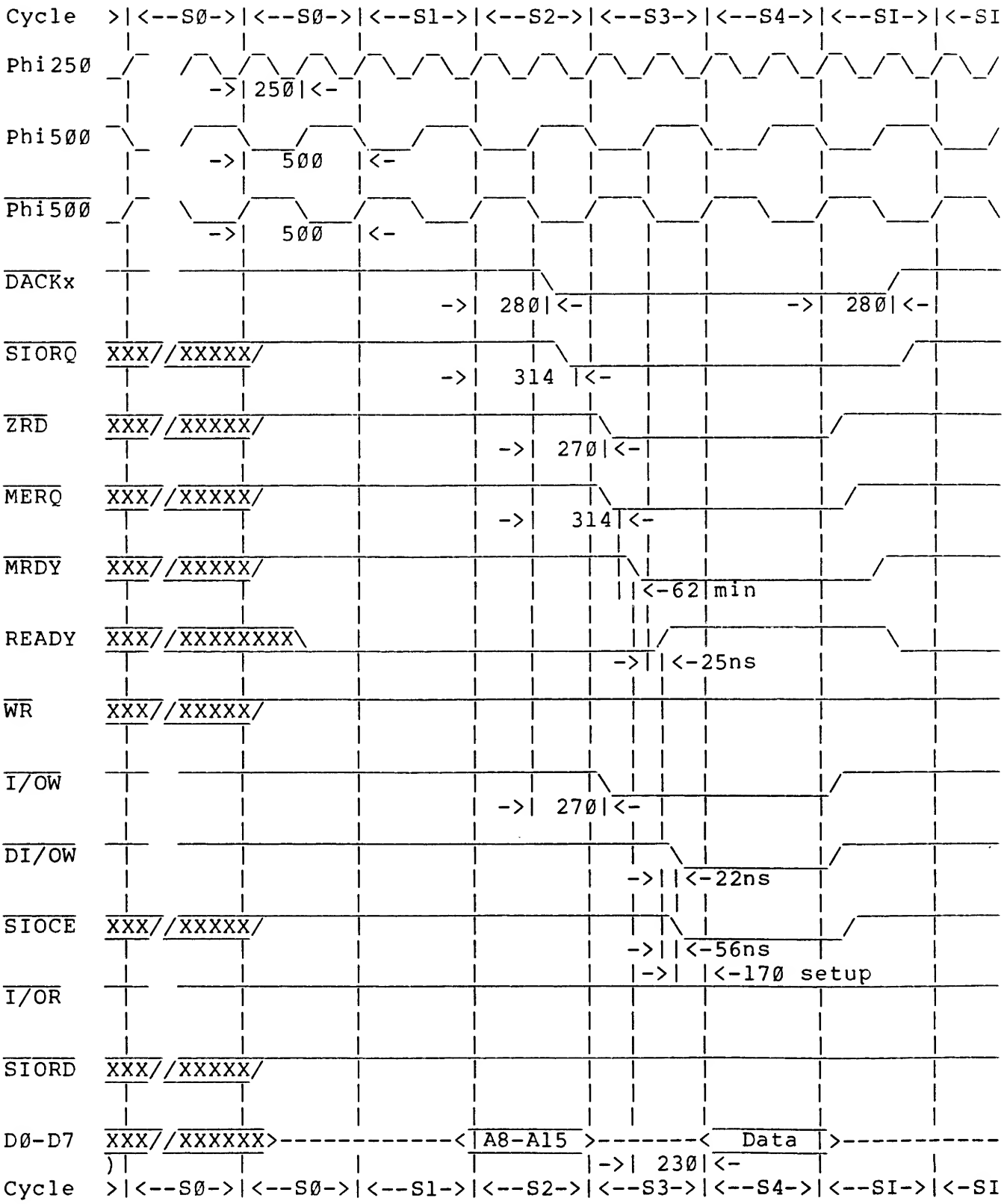
Scale: 62ns/sp



9517-DMA Controller (con't)

Data from Memory to SIO/2

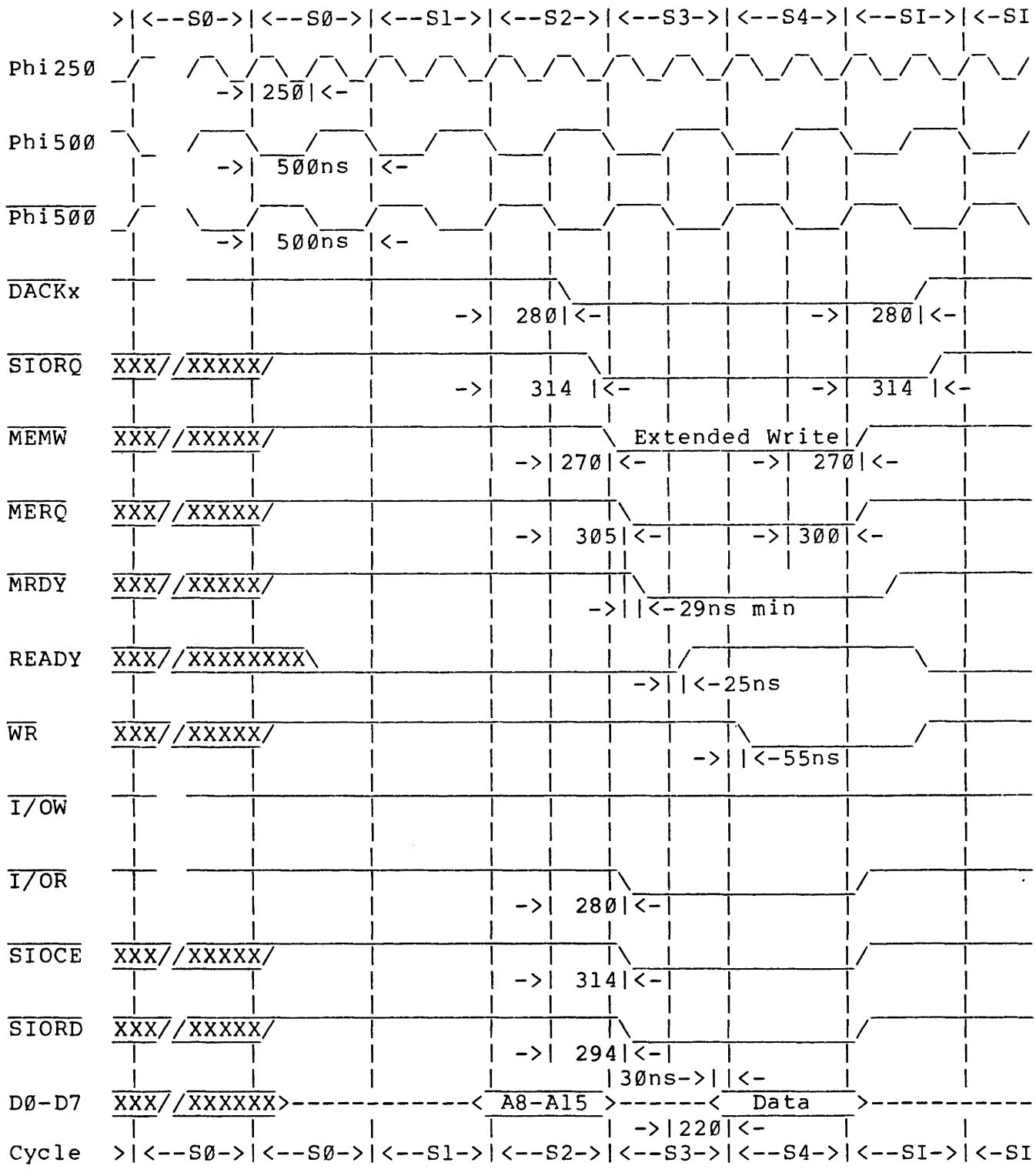
Scale: 62.5ns/sp



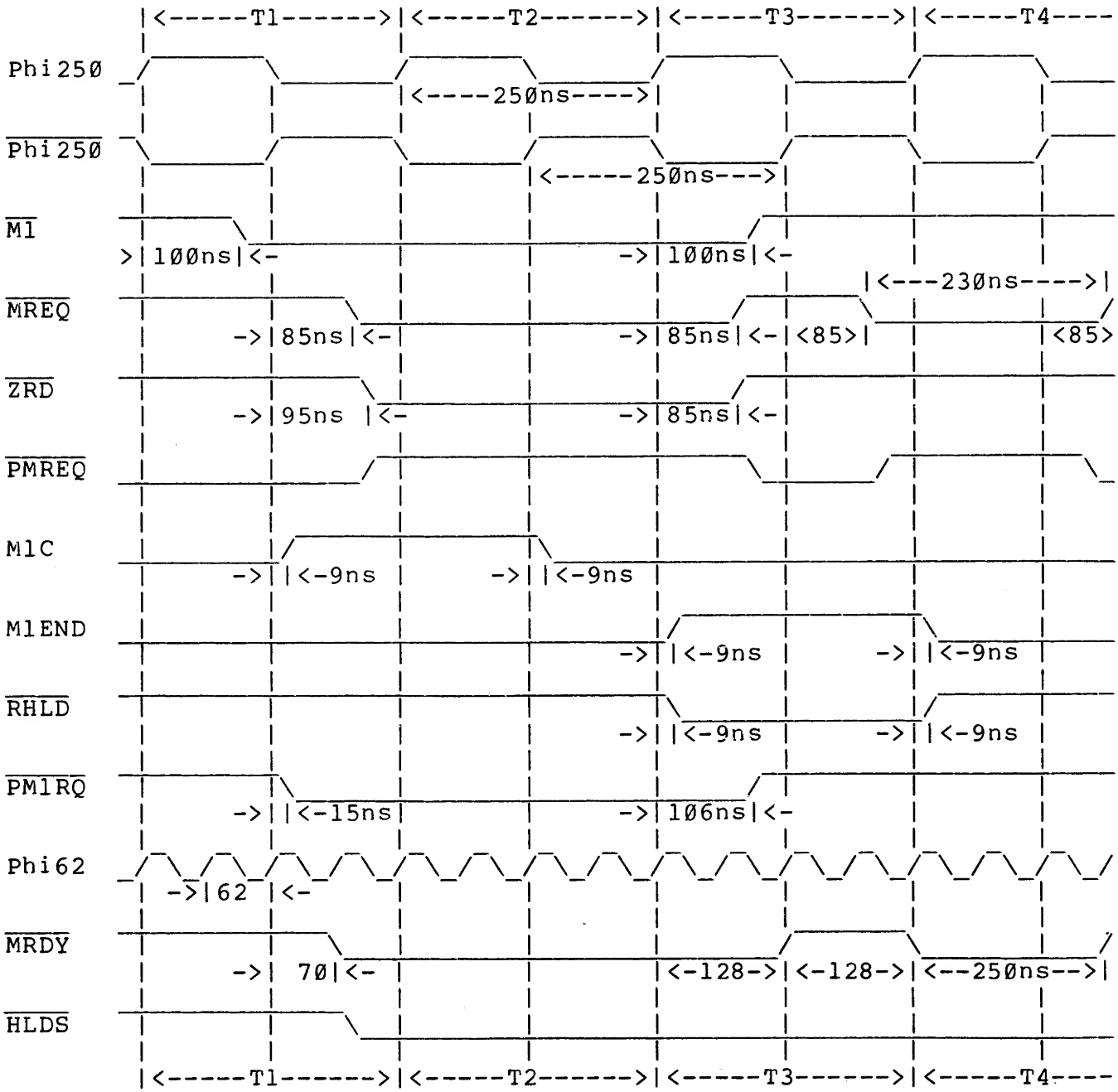
9517-DMA Controller (con't)

Data from SIO/2 to Memory

Scale: 62.5ns/sp



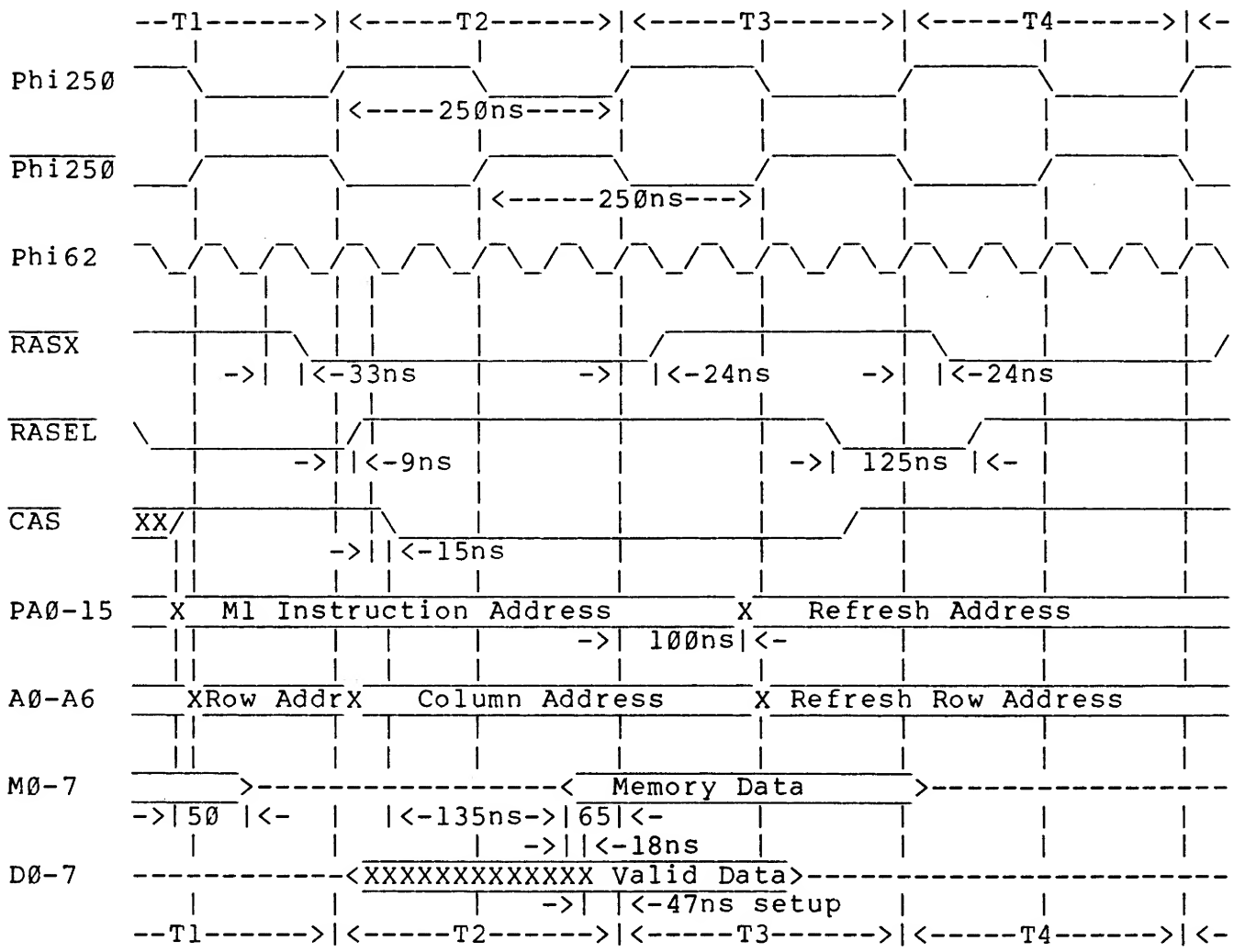
Memory Controller
CPU M1 Cycle Request
Scale: 15.6ns/sp



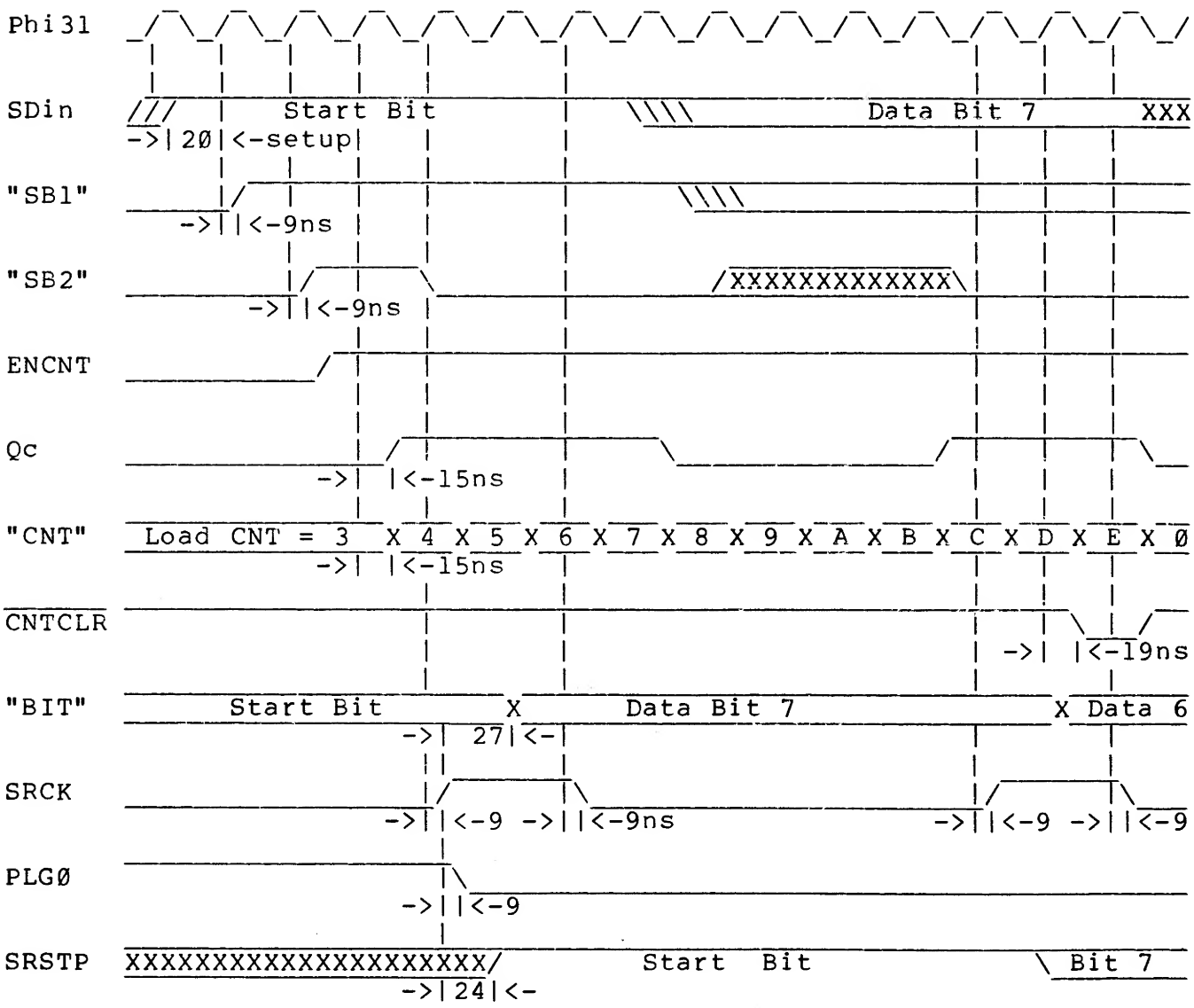
Memory Controller con't.

CPU M1 Cycle Request

Scale: 15.6ns/sp



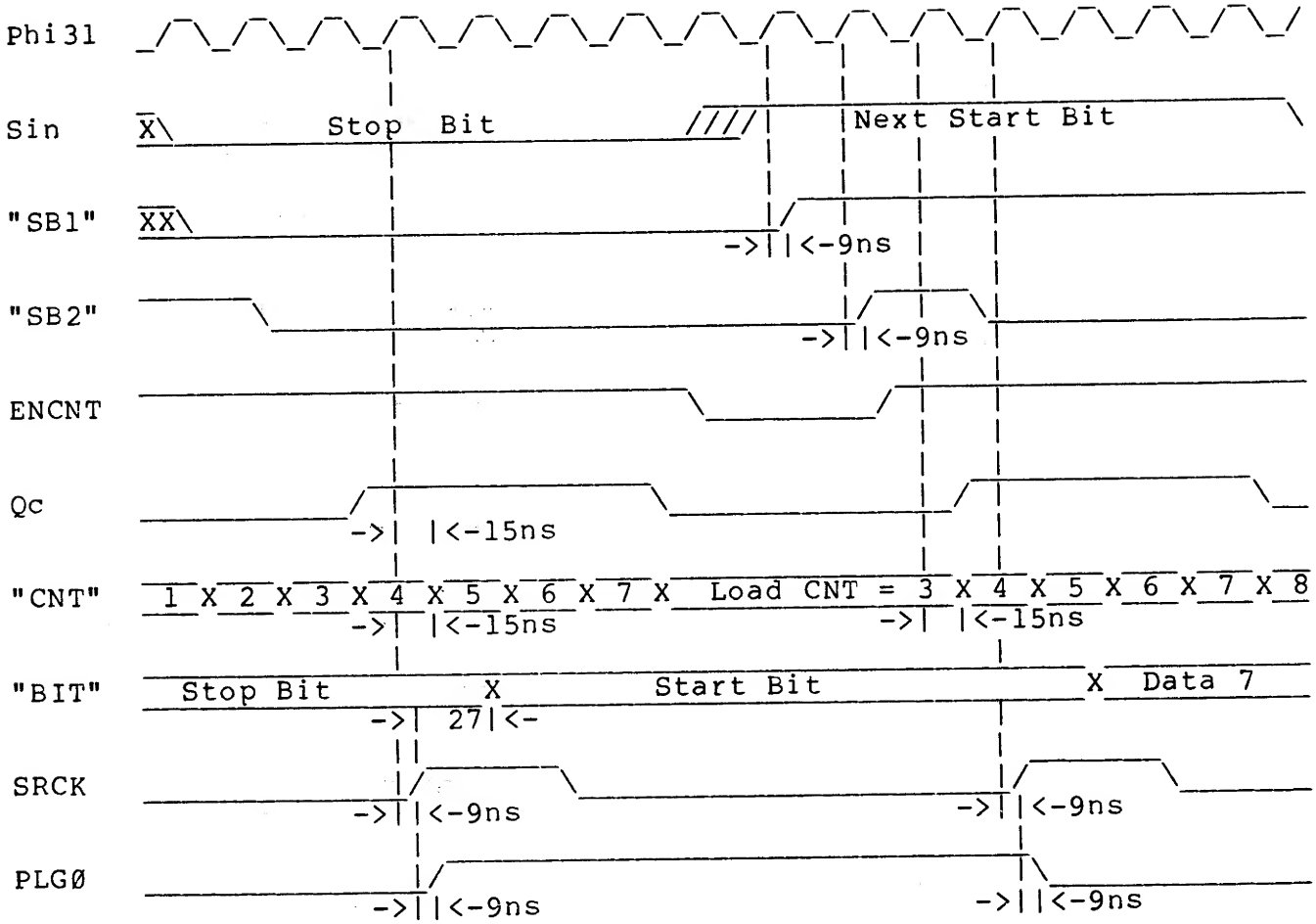
928 Data Link
Receiver Start Bit Synchronization
Scale: 7.83ns/sp



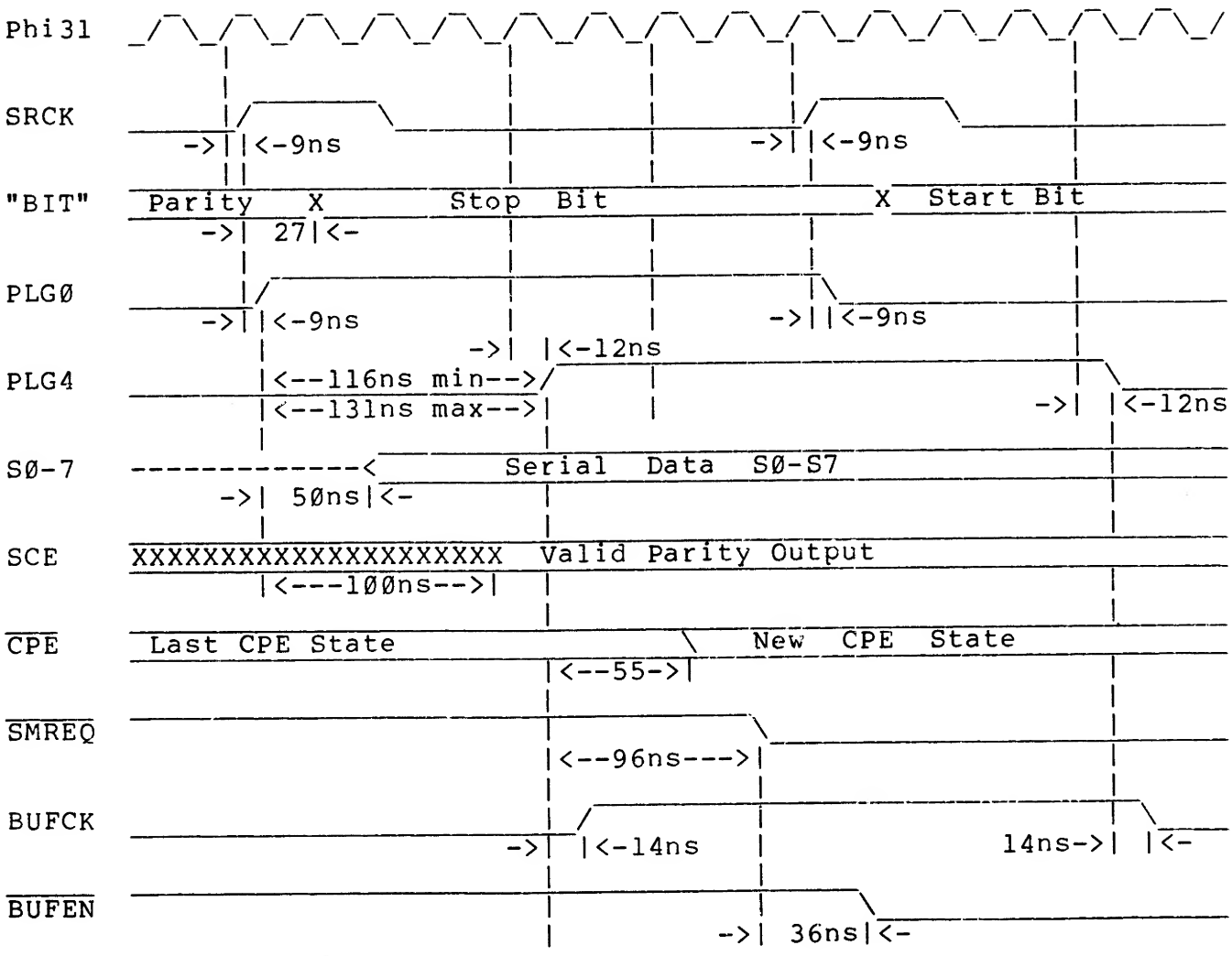
928 Data Link

Receiver Stop/Start Bit Synchronization

Scale: 7.83ns/sp



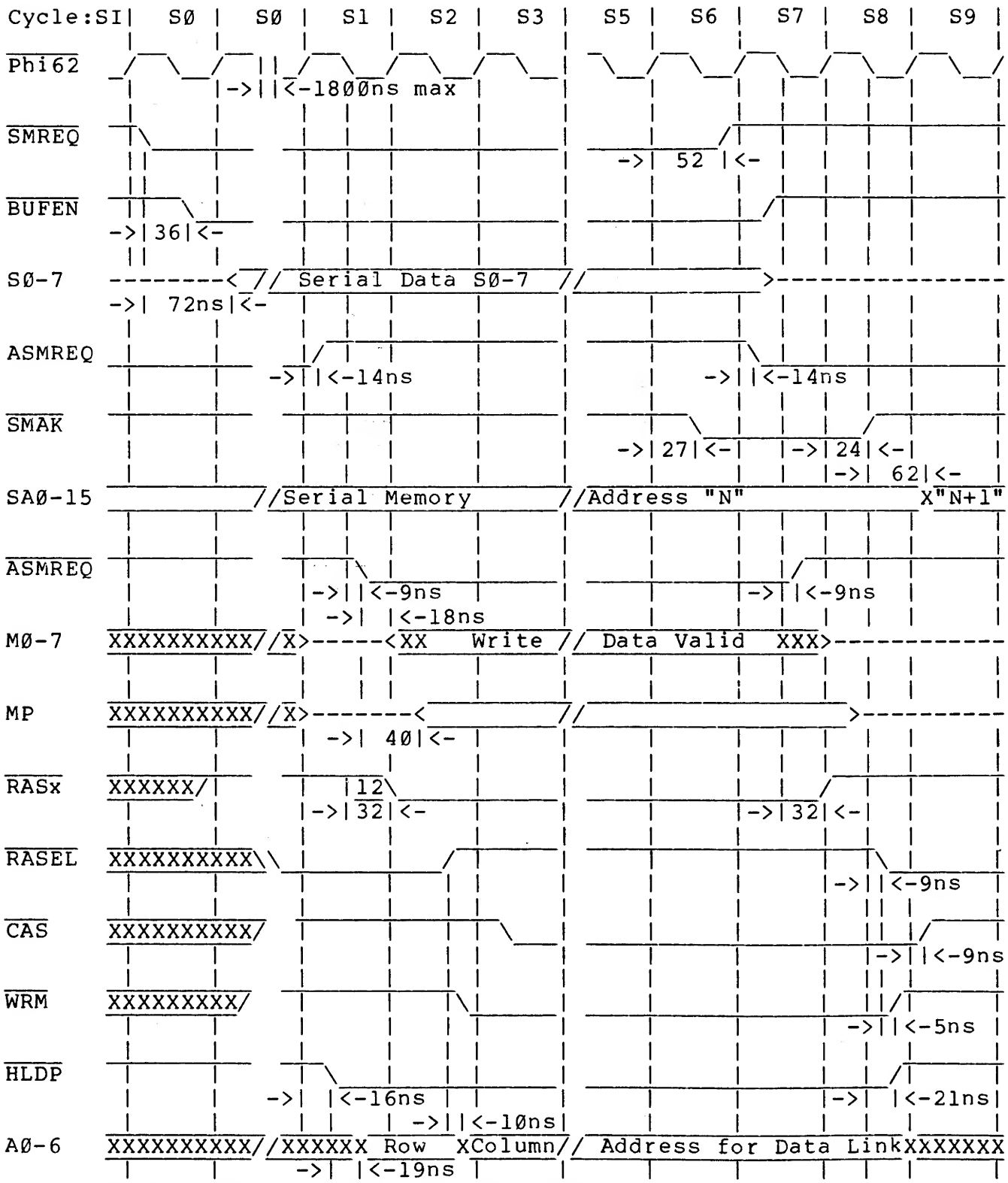
928 Data Link Receiver
Double Buffer Timing
Scale: 7.83/sp



928 Data Link Memory Interface

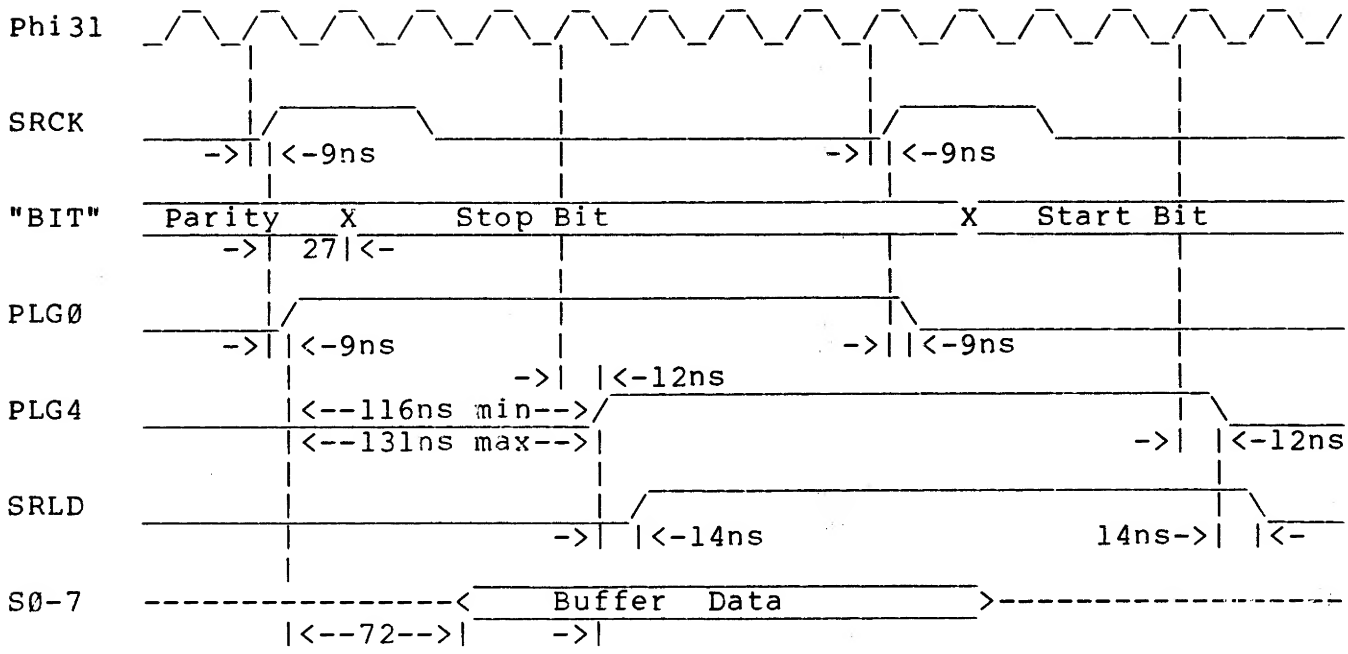
Write Timing

Scale: 10.4ns/sp



Note: MWT = 1, SWR = 0, and TRANS = 0.

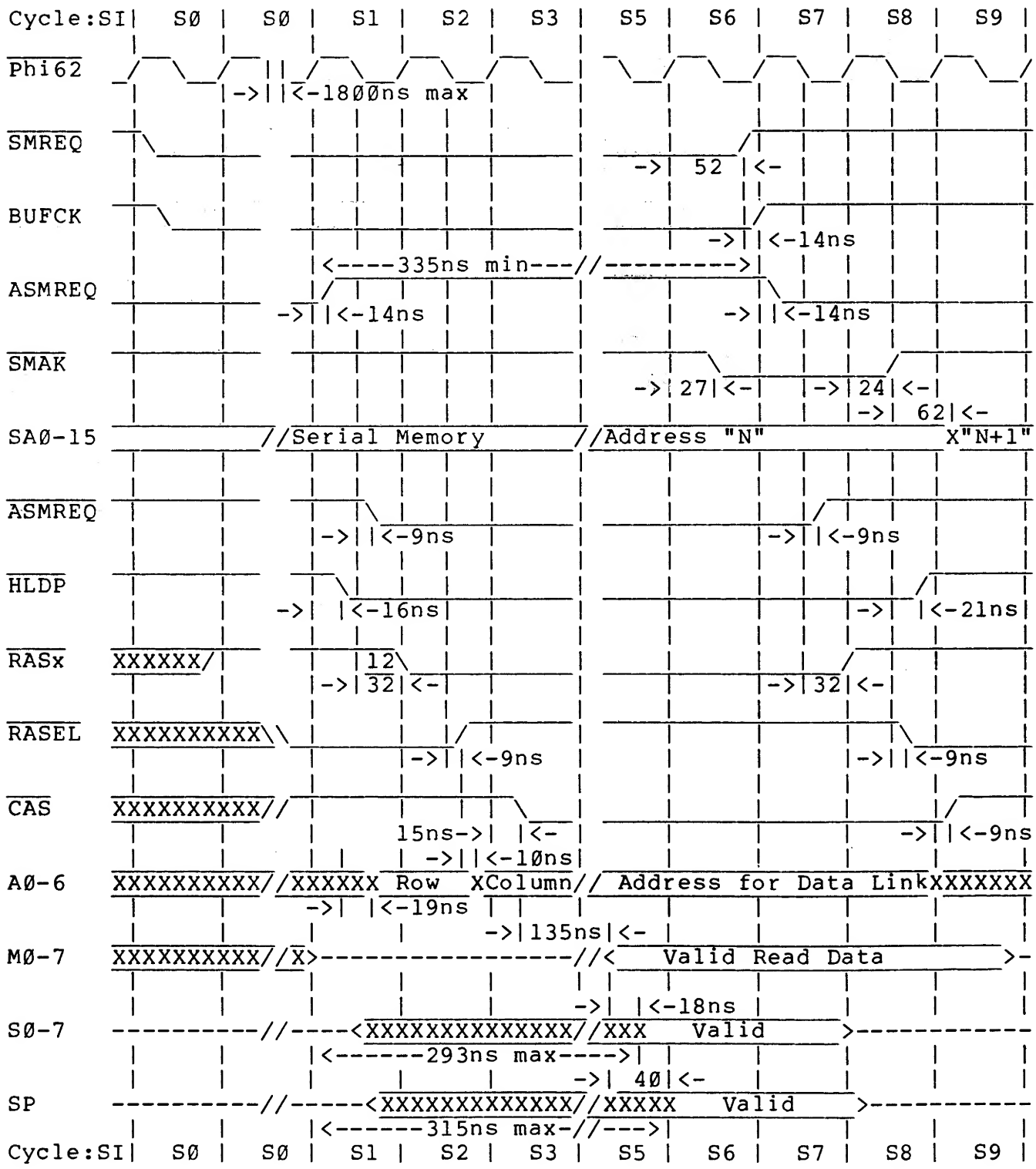
928 Data Link Transmitter
Double Buffer Timing
Scale: 7.83/sp



928 Data Link Memory Interface

Read Timing

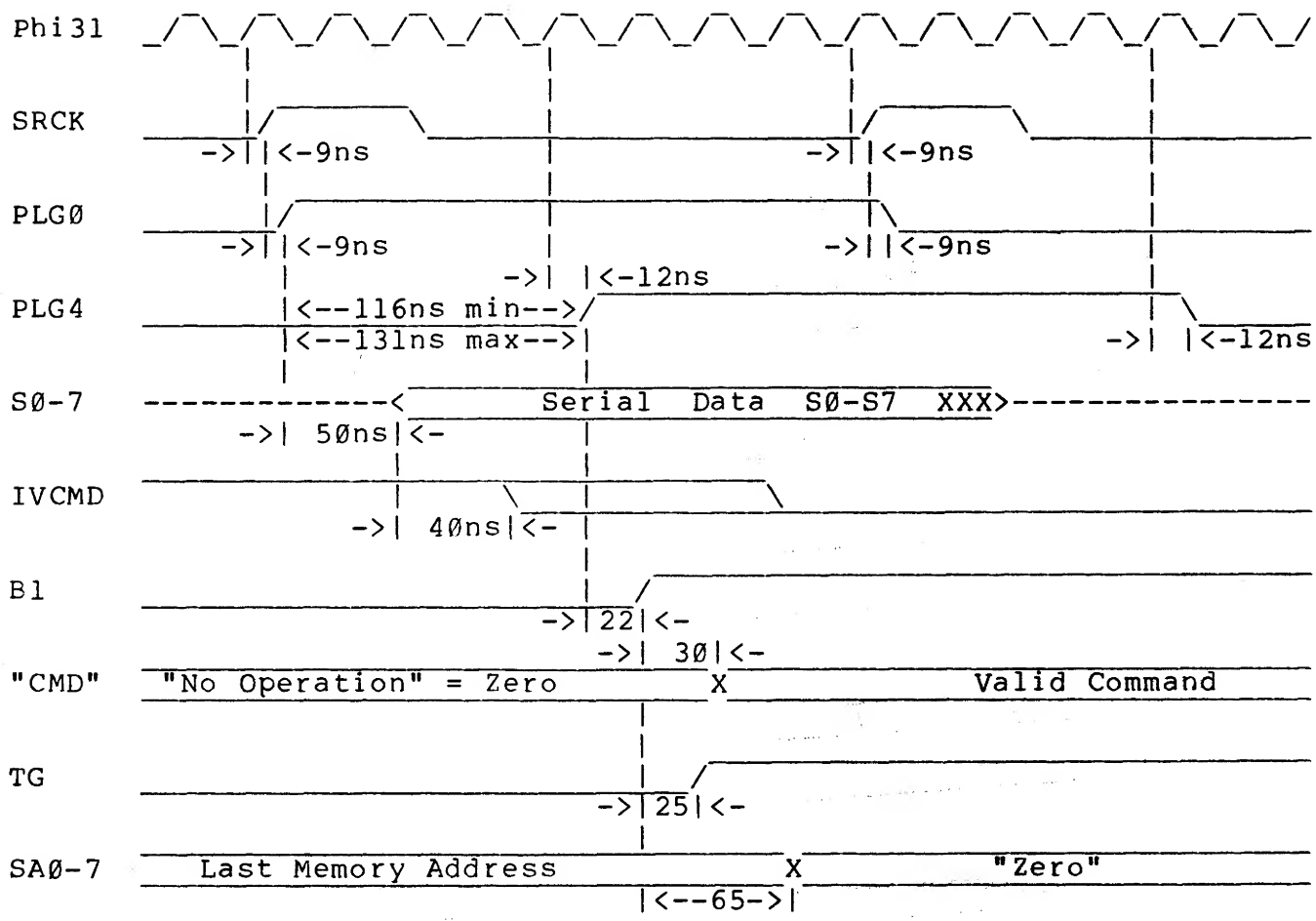
Scale: 10.4ns/sp.



Note: MWT = 0, $\overline{SWR}$ = 1, and TRANS = 1.

928 Data Link B1 State Timing

Scale 7.83ns/sp



WANG LABORATORIES, INC.

TO: Telecommunication Development Groups

FROM: R. M. Marston/Hsin Lin

DATE: May 21, 1981

SUBJECT: Changes to Telecommunications Processor (TCB-1) Specifications
ADDENDUM to HM 28

---

1. Section 2.17 (changes)

Address X '34' Control Register/"Deadman" Timer Control

Address X '35' Base Register, Monitor Block/Character Table

2. Section 12.2 (changes)

NB1, NB2, NB4, NB8, DPR, CRQ are active "low". (on = "ϕ" off = "1")

ACR, PND, PWI, COS, DOL, RI, TM, MPE, ZERO, SF/RF are active "high". (on = "1" off = "0")

3. Section 6.3 (addition)

The non-maskable interrupt (NMI) to the Z80 CPU is sourced from either the "Deadman timer" (ENMI see figure A) or "Latched Memory Parity Error" (LMPE see figure B). The selection of which source is accomplished by means of physical jumpers.

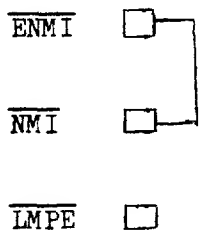


Figure A

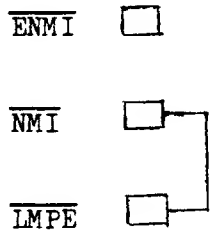


Figure B

0011E

T E C H N I C A L M E M O R A N D U M

H M 2 8

TO: Telecommunication Development Groups

FROM: Roger Cross

DATE: December 1, 1980

RE: Telecommunication Processor (TCB-1)

cc:

Ken Adams	David Anderson	Bernie Brady
Dan Bechar	John Campbell	Janet Carbone
Leo Chan	Bill Chittenden	Larry Conger
Stan Curtis	Mandy Davidson	Marigowda Divya
Bill Dressel	Don Dunning	Fritz Eberle
Len Ellis	Phil Florence	Mary Flynn
Suzanne Greenbaum	Paul Hackbarth	Jim Harmon
Rob Hawley	Mark Hewett	Bill Hutchins
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Harold Koplow	Ira Krakow	Hsin Lin
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rlc/0007c

INTRODUCTION

TELECOMMUNICATION PROCESSOR

Ø.1 Telecommunications for the Wang Systems will encompass a wide range of line disciplines and link protocols. To further this end, the TCB-1 Telecommunication Processor utilizes the following LSI components:

Z8ØA-CPU (4MHz clock operation), Z8ØA-SIO/2, Z8ØA-CTC, 9517A-DMA Controller (2MHz clock operation), and up to 64K bytes of Random Access Memory (MK4116-3).

Ø.2 The TCB-1 will also utilize a number of MSI components to provide:

928 Data Link; Power On Diagnostics; Memory Parity control; RS-232-C, and RS-449 MODEM interfaces; RS-366 Automatic Calling Unit interface; Character Recognition interrupts; 928 Data Link memory write access monitor; "Deadman" timer; and a TCB-1 Status Display panel.

PREREQUISITES

Ø.3 The following manuals and data sheets are required reading:

1) Z8ØA-CPU Technical Manual
2) Z8ØA-SIO Technical Manual
3) Z8ØA-CTC Technical Manual
4) AM9517A Direct Memory Access Controller
5) OIS System Operation OS-6
6) EIA Standard RS-232-C
7) EIA Standard RS-449
8) EIA Standard RS-366

Ø.4 Several other OIS System documents (TM documents) would be useful but are not required to understand this description.

GENERAL DESCRIPTION

1.Ø The Telecommunication Processor, hereafter referred to as the TCB-1, provides the flexibility to support almost any protocol and line discipline. The TCB-1 functional groups are a Processor section, Memory Controller section, and the 928 Data Link section. The Processor section contains the Z8ØA-CPU; Z8ØA-SIO/2; Z8ØA-CTC; RS-232-C, RS-449 and RS-366 interfaces; 9517A-DMA Controller; Character/928 Data Link (Master) monitor; "Deadman" timer; and TCB-1 Status display. The 928 Data Link section contains the coaxial line receive/transmit control, instruction and status/error control, and memory address/data control. The Memory Controller section coordinates TCB-1 memory access between the Processor section and the 928 Data Link section.

Processor Section

1.1 The central processing element, CPU, operates on a 25Ø.4 ns clock cycle. The CPU and the DMA Controller share a common bus, and use Bus Request/Bus Acknowledge to synchronize exchange of the bus control. Note: The DMA Controller operation will slow the Z8ØA-CPU execution, approx. 2 microseconds per byte.

1.2 The SIO/2 is controlled by the CPU and/or the DMA Controller; DMA allows very high speed communications (up to 88ØK bits per second) with minimal system overhead.

1.3 A CTC provides: a BAUD rate clock, a timer, and DMA Controller completion interrupts.

1.4 The communication interface allows either RS-232C or RS-449, program selectable, MODEM connections. The line encoding may be standard NRZ or NRZI, program selectable. The RS366 interface, standard for Automatic Calling Units (ACU), allows the TCB-1 to originate a communication session.

1.5 The Character/Master monitor enables the TCB-1 to monitor memory write accesses of the SIO/DMA and/or the 928 Data Link.

The monitor contains 1Ø24 (1K) bytes of Vector memory, which is shared between the Character and Master monitor functions.

1.6 The Character monitor allows the TCB-1 to conditionally generate a specific vectored interrupt if a program specified character is deposited by the DMA controller. The Character monitor uses a character recognition vector tables of 256 bytes in length. The system software may select any one of four vector tables to allow rapid context switching while processing a received data stream. The deposited character is used as an address to perform a "Lookup" in the program selected vector table. If the byte retrieved from the table has an LSB (VØ) of Ø, or the Monitor Control INTALL is on (see 9.7), an interrupt will be generated using this byte to form the Character vector. The Character Vector will always have V7 = 1 and VØ = Ø.

1.7 The Master monitor allows the TCB-1 to conditionally generate a specific vectored interrupt if a program specified memory address is written by 928 Data Link. The TCB-1 can monitor any 1k memory block, hereafter called the Monitor block, aligned on a 1k address boundary. The address (AØ-A9) in the Monitor block is used to retrieve a byte from Vector memory, if the MSB (V7) = Ø an interrupt will be generated using the retrieved byte to form the interrupt vector. The Master Vector will always have V7 = Ø and VØ = Ø.

1.8 The "Deadman" timer insures that the TCB-1 will not "Hang" the communications line in the event of a hardware/software fault. The timer will force Request To Send (RTS) into the inactive state if not reset by the system software every Ø.5 seconds or less. The timer may optionally force the CPU into the Non-Maskable interrupt service routine at location X'ØØ66' if the timer expires.

1.9 The Status Display provides signaling to a front mounted Light Emitting Diode (LED) display, this allows a varity of conditions to be displayed to the system operator.

928 Data Link Section

1.1Ø The 928 Data Link utilizes a dual coaxial cable to convey control and data information between the 928 Master and Slave Data Links. The channel, operated in half-duplex balanced mode, utilizes a high speed (4.275 M bits per second) START/STOP line discipline. The line format consists of eleven bit words containing: a Start bit, eight Data bits (SØ-S7), a Parity bit, and a Stop bit. The 928 Slave Data Link, under control of the Master Data Link (hereafter reffered to as "Master"), can respond to six different commands: two control commands, and four memory access commands. A summary follows:

928 Data Link Commands

1.11

Command	Action
RESTART	instructs 928 Data Link to RESET the Processor, clear IPL, MPE, and exit, if not already, Diagnostic mode
STATUS	instructs 928 Data Link to transmit the 928 Data Link and Processor status (CPE, IPL, MPE, etc.)
READ1	instructs 928 Data Link to transmit to the Master one byte from the specified TCB-1 memory address
WRITE1	instructs 928 Data Link to receive from the Master one byte and deposit it at the specified TCB-1 memory address
READ256	instructs 928 Data Link to retrieve from TCB-1 memory and transmit to the Master 256 bytes of data starting at the specified 256 byte aligned address
WRITE256	instructs 928 Data Link to receive from the Master 256 bytes of data and deposit it at the specified 256 byte aligned TCB-1 memory address

Memory Controller Section

1.12 The Memory Controller section coordinates memory access to TCB-1 memory. The memory space, organized as 8 bit bytes, may range between 16K and 64K bytes in 16K byte increments. The Memory Controller monitors requests from the 928 Data Link section and the Processor section on a round robin basis. Memory request are either granted by a READY notification or pended by a WAIT notification, thus allowing Processor and 928 data Link access interleaving. Note: 928 Data Link accesses will slow Processor execution. During a 256 byte page transfer, average reduction in Processor speed is 30%.

CPU Functions

2.0 The CPU is the main control and processing element of the TCB-1. Under direction of the system software, the CPU controls all functions of the TCB-1 except the 928 Data Link. The 928 Data Link, controlled by a Data Link Master, controls the Reset (RST), Initial Program Load (IPL) functions, and the Memory and Cable parity status/control. Programming the SIO/2, CTC, DMA Controller and the Character/Master monitor is the responsibility of the system software and is acomplished primarily by execution of IN and OUT (I/O) instructions.

2.1 The TCB-1 memory is both the control store and data store for the CPU. The CPU control store is loaded by the 928 Data Link and execution begins at address X'0000' after a 928 Data Link RESTART command. If a Memory Parity Error (MPE) is detected during execution the CPU is forced to execute "NOP's", the Status Display is set with Light Emiting Diodes (LED's) SL1-SL7 "ON" and SL8 blinking (see 17.0), and the 928 Data Link MPE status is set (see 2.1).

2.2 At Power-On time the TCB-1 enters diagnostic mode (see 15.0).

2.3 The TCB-1 interrupt scheme is standard for the Z80A family except for the Character/Master monitor and DMA Controller. The

Character/Master monitor does not require the "RETI" instruction execution at the end of the interrupt service routines and should only have a "RET" instruction. The DMA controller is not a Z80 family component, and instead uses Channel 2 and 3 of the CTC to signal interrupts.

2.4 The "Deadman" timer may use the Non-Maskable CPU interrupt and; if enabled, will interrupt any procedure or routine regardless of the interrupt mode or state of the maskable interrupt flag (see the Z80A-CPU Technical Manual).

2.5 Vectored interrupts (MODE 2) allow fast service and easy mapping of the service routines through the use of the "Vector" table. The maskable interrupt priority, from highest to lowest, for each device follows:

Vectored Interrupt Priorities

2.6	Highest	Character/Master Monitor		
2.7		SIO	Channel A	Receiver
				Transmitter
				External/Status
			Channel B	Receiver
				Transmitter
				External/Status
2.8		CTC	Channel 0	BAUD Rate Clock
			Channel 1	Timer
			Channel 2	DMA Controller 0/2 EOP
	Lowest		Channel 3	DMA Controller 1/3 EOP

2.9 The CPU controls the TCB-1 through the I/O functions, an I/O address summary follows:

CPU Input/Output Address Space

	Address	Device	Channel	Function	
2.10	X'00'	SIO	Channel A	Data Registers	
	X'01'		Channel B	Data Registers	
	X'02'		Channel A	Control Registers	
	X'03'		Channel B	Control Registers	
2.11	X'07'	Status/Address		Switches, input only	
2.12	X'10'	DMA	Channel 0	SIO Channel A	Current Address
	X'11'				Cur't Word Count
	X'12		Channel 1	SIO Channel B	Current Address
	X'13'				Cur't Word Count
	X'14'		Channel 2	SIO Channel A	Current Address
	X'15'				Cur't Word Count
	X'16'		Channel 3	SIO Channel B	Current Address
	X'17'				Cur't Word Count
2.13	X'18'		CONTROL	Write Command/Read Status Reg.	
	X'19'			Write Request Register	
	X'1A'			Write Single Mask Register Bit	
	X'1B'			Write Mode Register	
	X'1C'			Clear Byte Pointer Flip/Flop	
	X'1D'			Write Master Clear/Read Temp.	
	X'1F'			Write All Mask Register Bits	
2.14	X'20'	CTC	Channel 0	BAUD Rate Clock, IxC	
	X'21'		Channel 1	Timer	
	X'22'		Channel 2	DMA Controller, EOP Ch. 0/2	
	X'23'		Channel 3	DMA Controller, EOP Ch. 1/3	
2.15	X'30'	DMA	Write Next Receiver Ch. on DMA Cont. 0/2		
	X'31'		Write Next Transmitter Ch. on DMA Cont. 1/3		
2.16	X'32'		Update Curr. Receiver Ch. on DMA Cont. 0/2		
	X'33'		Update Current Transmitter Ch. on DMA 1/3		
2.17	X'34'	Monitor	Base Register, Monitor Block/Char. Table		
	X'35'		Control Register/"Deadman" timer Control		
2.18	X'36'	Deadman	Resets "Deadman" timer (out only, no data)		
2.19	X'37'	ACU	Autocall unit Control/Status register		
2.20	X'40	Line Interface & Status Switches	Write Line Controls/Read Address/Status Switches		
2.21	X'50'	Diagnostics	Exit Diagnostic Mode		
	X'51'	OUT only,	Enable Memory Parity Generator		
	X'53'	no data	Disable Memory Parity Generator		
2.22	X'60'	928 Type	Read 928 Device Type		
2.23	X'70'	Status Display	Write TCB-1 Status Display		

2.24 I/O addresses not explicitly described above should not be selected, since device addresses are only partially decoded and device confusion will result.

SIO/2 Functions

3.Ø The SIO/2 element, operating on a 4MHz (25Ø.4ns) clock, converts data from 8 bit parallel format to one of several serial formats and vice versa. In addition, the SIO/2 performs character and line buffering; line control and status monitoring; and error protection and detection. Both Synchronous and Asynchronous line displines are supported. Synchronous mode supports both Bit Oriented Protocols (BOP's) and Character Oriented Protocols (COP's). Asynchronous mode (Start/Stop) allows variable data, stop bit, and parity fields. The Z8ØA-SIO Technical Manual contains a complete description of the various modes and line disciplines.

3.1 The CPU controls the SIO/2 functions by I/O instructions as outlined in 2.1Ø. The CPU may also select data line encoding, NRZ to NRZI conversion, and internal or external BAUD rate clock by OUTPUT to the Line Control Register (see 13.Ø).

3.2 Within the SIO/2, Channel A is configured as the Receiver and Channel B as the Transmitter; this configuration allows fullduplex DMA operations by using the WAIT/READY function of each channel. Channel A DMA request (W/RDYA) may be routed to either Channel Ø or Channel 2 of the DMA Controller. Equivalently, Channel B (W/RDYB) may be routed to either Channel 1 or Channel 3 of the DMA Controller (see 4.2). Two SIO/2 inputs, DCDB and CTSA, are used to monitor MODEM signals Data Set Ready (DSR) and Ring Indicator (RI), respectively. Channel A's Transmitter is looped back into Channel B's receiver for diagnostic use.

3.3 SIO/2 Controls

Control	Type	Function
TxCA	Input	Internal Clock (IxC) derived from CTC Ch. 1
RxCA	Input	Reciver Clock, selectable Internal/External
DCDA	Input	Carrier Detect from MODEM (DCD)
RxDA	Input	Received Data from MODEM
RTSA	Output	not used
CTSA	Input	Ring Indicator (RI)
TxDA	Output	looped back to RxDB
TxCB	Input	Transmitter Clock, selectable Int/Ext
RxCB	Input	Internal Clock (IxC)
DCDB	Input	MODEM Data Set Ready (DSR)
RxDB	Input	looped back from TxDA
RTSB	Output	Request To Send (RTS),
CTSB	Input	Clear To Send (CTS)
TxDB	Output	Data Transmited to MODEM
W/RDYA	Output	request DMA Controller Channel Ø/2 service
W/RDYB	Output	request DMA Controller Channel 1/3 service
RESET	Input	Processor RESET or Memory Parity Error

9517A-DMA Controller

4.Ø The DMA Controller, operating on a 5ØØ.8ns clock, allows high speed data transfer between the SIO/2 and TCB-1 memory. The CPU controls the function of the DMA Controller through I/O instruct- ions as outlined in 2.12, 2.15, and 2.16.

4.1 The SIO/2 Receiver (Channel A) and Transmitter (Channel B) are double buffered by the DMA controller and the associated circuits. Channels Ø and 2 support data input for the SIO/2 Receiver and are called the Receiver Channel pair, likewise, Channels 1 and 3 support data output for the SIO/2 Transmitter and are called the Transmitter Channel pair.

4.2 The Next and Current Channel Registers, one set for each DMA Channel pair, control the routing of the SIO/2 DMA requests to one of the channels in the pair (these are external registers not inside the DMA Controller). When an End Of Process (EOP) is signaled by the DMA Controller for a particular channel pair, the Next Channel Register is copied into the Current Channel Register effectivly switching to the next desired channel; in addition the CTC will signal an interrupt for that pair.

4.3 This type of channel switching allows the system sofware to set the Next Channel Register to the inactive channel of that pair, program all the required register values for the next desired memory buffer, and then unmask the channel to await EOP on the active channel. When the EOP occurs, the "Next" is copied to the "Current" register, W/RDYx is routed to the previously inactive channel and future requests are honored by the newly selected channel.

4.4 The DMA Controller options must be set for Extended Write, DACK outputs active LOW, DREQ inputs active high, single byte transfer mode, and rotating DREQ priority.

4.5 CTC Channels 2 and 3, Clock/Trigger inputs, monitor the DMA Channel pairs Ø/2 and 1/3, respectively, for an EOP. The CTC should request an interrupt if either of the inputs go low (=Ø) and provide the "Vector" during Interrupt Acknowledge (see 5.Ø).

CTC Functions

5.Ø The CTC provides the TCB-1 with timing and counting functions. Channel Ø, with a Clock/Trigger input of 2MHz (5ØØns), is used to generate an Internal Clock (IxC) which may be routed to the SIO/2 Receiver and/or Transmitter. Channel 1 is used for software event timing. Channel 1's Clock/Trigger input is IxC generated by Channel Ø; this allows Channels Ø and 1 to operate in a cascaded mode. Channels 2 and 3 are used to alert the CPU of DMA completion (see 4.5).

5.1 The CTC is programmed by the CPU and is mapped in the I/O space as outlined in 2.14. Channel Ø may programmed for either counter mode or timer mode depending on the desired BAUD rate. The ZC/TOØ output (Channel Ø) rate is divided by two to produce a 5Ø/5Ø duty cycle Internal Clock (IxC). This clock is supplied to the SIO/2, the RS-232-C interface (pin 11), CTC Channel 1, and to the Internal/External Clock selector (see 13.Ø). The RS-449 interface may selectively emit, on the TT signal, either the external clock (ST) or the Internal Clock (IxC) (see 13.Ø). Channel 1 may be programmed for either timer mode or counter mode

operation to generate an interrupt on each time-out. Timer mode allows a number of system clock cycles (16*N, or 256*N, where 1<=N<=256) to expire before generating each interrupt, while Counter mode counts a number (1<=N<=256) of IxC clock cycles before generating each interrupt. Channels 2 and 3 monitor the DMA Controller's EOP signal for each Channel pair and should both be programmed for count mode operation to interrupt on a single falling edge of the Clock/Trigger input.

Deadman Timer

6.Ø The "Deadman" timer prevents the communications line from being "jammed" by the TCB-1 in the event of a software/hardware failure. The CPU controls the "Deadman" timer functions through I/O instructions as outlined in 2.17 and 2.18. Two control bits, DNMI and DDMT, are provided to select the timer options and are concatenated with the Monitor Control bits (see 9.2). The timer must be used whenever Request To Send (RTS) is to be presented to the MODEM. It may also be used as a general software time-out device to produce a Non-Maskable Interrupt. Once enabled, the timer should be periodically reset by the system software at least every Ø.5 seconds to prevent its expiration (approx. Ø.7 seconds).

6.1 If DNMI is set to one, the CPU will not be interrupted regardless of the state of the "Deadman" timer. If DNMI is set to zero, the CPU will be unconditionally interrupted when the timer expires, via Non-Maskable Interrupt (NMI) to X'ØØ66'. The DNMI bit should only be set to one, disabling the NMI, before the DDMT (see 6.2) is set (=1) to disable the timer. It should only be reset (=Ø) after the DDMT is reset (=Ø), to enable the timer (i.e. the DNMI state change should always be bracked by the state change in DDMT). If the "Deadman" interrupt is enabled, Vector memory will be mapped out of the Processor memory space when the interrupt (NMI) is active (timer has expired), regardless of the state of MAPOUT. This prevents NMI instructions (at X'ØØ66') from being fetched from Vector Memory mapped in at X'ØØØØ'.

6.2 DDMT enables the "Deadman" timer. Setting DDMT to one will stop the timer function and disable the RTS signal to the MODEM. If the NMI function is being used it must be turned off before the timer is disabled. Setting DDMT to zero will start the timer and allow a RTS signal to be presented to the MODEM. If the NMI function is desired, it must be enabled (=Ø) after the DDMT bit is reset (=Ø).

Character and Master Monitors

7.Ø The Character and Master monitors provide supervisory services for the TCB-1. Each monitor alerts the CPU if a specific memory write occurs. The Character monitor "watches" characters deposited by the DMA controller, while the Master monitor "watches" the 928 Data Link memory write accesses. Each monitor may "watch" for several different events, simultaneously (up to 1Ø24).

7.1 The Character monitor allows the TCB-1 to process Binary Synchronous Communication (BSC) protocols with a minimum of system overhead; but its uses are not limited to the BSC class. The Character monitor can interrupt the CPU when any specific characters (control, format, etc.) are deposited in memory. Thus, the CPU can perform an immediate action such as disabling the Receiver CRC, switch DMA buffers, etc..

7.2 The Master monitor can interrupt the CPU when specific memory addresses are write accessed by the "Master". This "Master" interrupt can be used to queue another request, awaken a sleeping task, etc.. The monitors share the Control register, the Base register, the First In First Out memory (FIFO), and the 1Ø24 byte Vector memory.

Monitor FIFO

8.Ø The Monitor First In First Out memory (FIFO) may hold up to sixteen vectors awaiting CPU acknowledgement. Either monitor may deposit vectors in the FIFO. In the event of a FIFO overflow,

either a X'ØØ' or X'8Ø' vector will be deposited in the FIFO to indicate which monitor was the last to overflow (this does not mean that only one monitor overflowed but that it was the last one to overflow). Therefore, Vectors X'ØØ' and X'8Ø' are reserved and should not be used by other devices. As Vectors are deposited in the FIFO the LSB, VØ, will be reset to zero and the MSB, V7, will be set to reflect which monitor acted in the deposition. VØ = Ø assures that all Interrupt Service Routine Program Counters are aligned on a halfword boundaries. V7 = 1 indicates a Character monitor vector, while V7 = Ø indicates a Master monitor vector.

Monitor Control Register

9.Ø The Monitor Control register contains eight control bits, six of which determine the mode of monitor operation. The two remaining bits control the "Deadman" timer. The CPU controls the contents of the Monitor Control register which is mapped in the I/O space as outlined in 2.17. The contents of the Monitor Control register are all set (=1) at Processor RESET time. The Control bits have the following configuration:

Monitor Control Register Format

9.1

Data Bit Position	Control Bit Name	Function
DØ	MAPOUT	Removes Vector memory from Processor memory space
D1	CHARMON	Enables Character monitor function
D2	MASMON	Enables Master monitor function
D3	CLRINT	Clears all pending interrupts
D4	INTALL	Forces VØ = Ø, generates interrupt on all characters
D5	BUFOFF	Disables buffering by SIO-DMA pair
D6	DNMI	Disables "Deadman" NMInterrupt
D7	DDMT	Disables "Deadman" timer

9.2

MAPOUT

9.3 The Vector memory may be selectively mapped into the Pro-

cessor memory space by this bit. When set to zero, the Vector memory appears at the address contained in the Monitor Base register (upper six bits only). When set to one, the Vector memory is removed from the Processor memory space. The state of MAPOUT may be changed at any time, regardless of other Monitor Control bit states.

CHARMON

9.4 The Character monitor may be selectively enabled or disabled by this bit. When set to one, the characters deposited by the DMA controller are "Looked-Up" in the Vector memory to see if a CPU interrupt is required. The bit state may be changed at any time and does not affect vectors previously stored in the monitor FIFO.

MASMON

9.5 The Master monitor may be selectively enabled or disabled by this bit. The Master monitor is active when this bit is set to one. The bit state should only be changed when the 928 Data Link is polling or inactive (i.e. not while 928 Data Link may be writting in the monitor block). Changing the bit's state has no effect on vectors previously stored in the monitor FIFO.

CLRINT

9.6 The monitor FIFO may be purged by this control bit. After the CPU interrupts are disabled, this bit may be set to one to discard all pending interrupts and allowed no other interrupts until the bit is reset. CLRINT may be reset (=Ø) any time except when the MASMON bit is enabled (=1), in this case it may be reset when the 928 Data Link is polling or inactive (i.e. not writing in the monitor block).

INTALL

9.7 When set to one, this bit forces VØ to zero when a character is "Looked-Up" in Vector memory. Therefore all characters generate interrupts regardless of the value of VØ in Vector memory. INTALL allows easy handling of paired control characters. The state of this bit may be changed at any time, regardless of the state of any other monitor control bits.

BUFOFF

9.8 This bit is used to control DMA controller write access (Channels Ø and 2) to TCB-1 memory. If this bit is set (=1), no restrictions are placed on the DMA controller memory access and transfers are made as soon as the character is loaded in the SIO/2 Receiver FIFO. If this bit is reset to zero, the DMA controller write access is prohibited when a Character Vector is loaded in the monitor FIFO. After the vector is acknowledged, the access is restored by the first DMA controller I/O access (by the CPU) in the Character Interrupt Service routine. Therefore, the DMA controller must wait for the Character Vector to be passed to the CPU (entry to the service routine) and then for the CPU to access any DMA control register. This will allow information to be retrieved from, or provided to, the DMA controller concerning either the character that was just deposited or the next character in the SIO/2 Receiver. Only one CPU I/O access is allowed before the DMA controller memory access is restored. If the information transfer requires more than one I/O access, the channel request, DREQx, should be masked to prevent a waiting request from being serviced and disturbing the state of the channel registers.

Monitor Base Register

10.Ø The Monitor Base register contains the 1K block address for Vector memory. It also indicates the area in TCB-1 memory which

is used for communications with the "Master", hereafter called the Monitor block. Only the six most significant bits are used in the block address recognition process. The remaining two bits are used in the Character monitor to select the recognition table. The CPU controls the contents of the Monitor Base register which is mapped in the I/O space as outlined in 2.17.

10.1 Note: The Monitor Base address (upper six bits, MBA10-15) should not be changed while the Master monitor is enabled, although the lower two bits (MBA8 and MBA9) may be changed any time.

Vector Memory

11.0 The Vector Memory contains information to determine which memory events should generate interrupts and the vectors that are passed to the CPU to indicate which events occured. The memory is shared between the Character and Master monitor. It consist of two 4 X 1024 bit static memories (2114-A's) arranged as 1024 eight bit bytes. The Vector Memory bits are referred to as V0-V7, with V0 being least significant.

11.1 V0 = 0 activates a location as a potential Character Vector, and V7 = 0 does likewise for a Master Vector. V7 is set to indicate which process caused the vector to be deposited in the FIFO (Character = 1 and Master = 0). The remaining bits, V1-V6, are passed on as they were programmed in Vector Memory. With the above constraints, a single Vector Memory location may be shared between the two monitors.

11.2 The Vector Memory may be mapped into the Processor memory space at the address loaded in the Monitor Base Address register (see 10.0). Access to the Vector Memory has no effect on TCB-1 memory normally found at the same address. Vector memory is transparent to the 928 Data Link and does not affect its TCB-1 memory access. When the Vector memory is mapped into the memory space, the CPU may perform any type of memory access (such as Read cycles, Write cycles, even M1 Instruction Fetch cycles; although M1 cycles are not reccommended and care should be used when mapping in Vector Memory not to attempt to access TCB-1

memory normally found at the Vector memory address).

11.3 The Vector Memory has the lowest access priority. For example, if the Vector Memory were mapped in at the same location as Diagnostic PROM (X'FØØØ'-X'FFFF' when in Diagnostic Mode) the Memory Read Cycle would select PROM, while the Memory Write cycle would select Vector Memory. If the "Deadman" timer interrupt is enabled (DNMI), Vector Memory access will be inhibited if the timer has expired; this prevents instructions from incorrectly being fetched from Vector Memory (in the event that Vector memory is mapped into the Processor space at X'ØØØØ'-X'Ø3FF').

11.4 The Vector Memory is interrogated for each memory cycle. If a DMA Controller Write cycle is active, the Vector Memory address is created from the data word (character) being stored(i.e. a direct memory lookup). Since a character is only eight bits, the remaining two bits (1Ø bits in all) are taken from the least significant positions of the Monitor Base register, thus allowing one of four different tables, of 256 bytes each, to be used in the lookup process (MBA8 and MBA9 are table select bits).

11.5 The character lookup address mapping is:

D0 = VA0, D1 = VA1, D2 = VA2, D3 = VA3, D4 = VA4,D5 = VA5, D6 = VA6, D7 = VA7, MBA8 = VA8, and MBA9 = VA9

Where DØ-D7 is the character value, MBA8 and MBA9 are table select bits, and VAØ-VA9 is the Vector Memory address value obtained.

11.6 VØ of the vector obtained from the above address is checked and if zero the vector is placed in the monitor FIFO. The FIFO will then request an interrupt of the CPU. Alternately, the VØ bit may be forced to zero by setting INTALL, a control bit in the monitor control register, which causes all characters to generate an interrupt (useful in paired control character cases, e.g. DLE SYN).

11.7 The Master monitor operates on a selected area of TCB-1 memory. Any one kilo-byte (1K) memory block, which resides on a 1K address boundary, may be "watched". The memory block, hereafter called the Monitor Block, is specified in the Monitor Base

register. The Vector memory has a one to one address correspondence to this block. During a 928 Data Link Write access, if V7 of the Vector obtained from Vector memory is zero the Vector is deposited in the monitor FIFO. The FIFO will present an interrupt request and pass the vector to the CPU during Interrupt Acknowledge. Any number of bytes in the 1K block may be "watched". In some systems, monitoring the semaphore bytes, which indicate that a service has completed and that another may be started, would be ideal use of the Master monitor. In this case, a "Pipe Line" operation could be established to provide fast "Master" services.

Automatic Calling Unit (ACU)

12.Ø The RS-366 ACU Interface allows the TCB-1 to orignate dialed calls. The CPU controls this interface through the I/O instructions as outlined in 2.19. The MODEM signals RI or IC, and TM; and the Memory Parity Error register (MPE) are appended to the status register. The SF/RF MODEM signal (see RS-449) is appended to the control register. The format of the Control/Status register follows:

ACU Register Format

12.1

Data Bit	Ø	1	2	3	4	5	6	7
Control	NB1	NB2	NB4	NB8	DPR	CRQ	zero	SF/RF
Status	ACR	PND	PWI	COS	DLO	RI	TM	MPE

Note: All bits are positive logic; ON=1; OFF=Ø.

Line Interface

13.Ø The Line Interface register allows the TCB-1 to select Internal or External SIO/2 Receiver clock, Internal or External SIO/2 Transmitter clock (the RS-449 signal TT is identical to the SIO/2 Transmitter clock), NRZI or NRZ line encoding, and RS-449 or RS-232C interface. The CPU controls the Line Interface Reg-

ister through I/O instructions as outlined in 2.20. Only Data Bits 0-3 are used, the others should be set to zero.

Line Control Register Format

13.1

Data Bit	0	1	2	3
Control Select	Rx INT/EXT 1 = EXT	Tx INT/EXT 1 = EXT	NRZI/NRZ 1 = NRZ	RS-449/232C 1 = 232C

Address/Status Switches

14.0 The Address/Status switches enable the TCB-1 to obtain configuration information. The eight switch settings could be an address within a network or a status indicating an expected TCB-1 operation. Therefore, the switch settings are software specified. The switch settings are obtained by a CPU IN instruction and is mapped, twice for software compatibility, in the I/O space as outlined in 2.11 and 2.20. The ON position is Binary 1, Switch 1 is Data Bit 0, Switch 2 is Data Bit 1, etc..

Diagnostic Functions

15.0 The TCB-1 provides several diagnostic functions. The Memory Parity Generator may be controlled by the CPU through OUT instructions as outlined in 2.21. If the Memory Parity Generator is disabled:

15.1
1) Fixed Parity is written to memory (Parity Bit=1) for all subsequent memory write accesses.
2) The status of the MPE register is inhibited in the 928 Data Link Status register.
3) The SIO/2 is not RESET on MPE error detection.
4) The CPU is not forced to execute "NOP's" on MPE error detection.

15.2 Memory Parity Error (MPE) may be examined by a CPU Input instruction from the ACU Status register (see 12.0). MPE may be cleared (MPE = 0) by setting or resetting the Memory Parity mode.

15.3 At Power-On time, the Processor section is RESET and the 928 Data Link transmitter is disabled (although the 928 Data Link

receiver remains functional). The CPU begins execution of forced "NOP's" at X'0000' (see 15.3) until it reaches instruction address X'F000', which triggers the TCB-1 into Diagnostic Mode and 4K bytes of EPROM (2716) is mapped into the memory space at address X'F000'. In the Diagnostic mode "forced" Memory Parity Error "NOP's" are inhibited.

15.4 If the diagnostics are completed the Status Display should be set to indicate the TCB-1 Status and the CPU should Exit Diagnostic Mode by an Output instruction (see 2.21). The EPROM will be mapped out of the memory space, and the 928 Data Link transmitter enabled. "NOP's" will be executed until the 928 Data Link deposits the control store and signals RESET. Otherwise, the Diagnostic status should be set and the CPU "HALT'ed".

15.5 The "Master" may terminate the TCB-1 Diagnostic mode by sending RESTART to the 928 Data Link. This may cause problems in some systems if the Power-On Diagnostics are to be reexcuted, therefore it is recommended that the coaxial cables be disconnected in this case. The primary advantage in allowing the 928 Data Link to force an exit from Diagnostic mode during debugging, where the current program is to be purged by the RST button (on the front panel) and new code is to be loaded. Sometime after depressing the RST button, the "Master" will attempt to poll the TCB-1's SCA area; the 928 Data Link transmitter is disabled and the poll fails. The "Master", after several attempts belives the TCB-1 is "Dead", and will attempt to revive it by "Bootstraping" (IPL) ; the resulting RESTART command forces Diagnostic mode exit and normal program excution at X'0000'.

928 Device Type Switches

16.0 The 928 Device Type switch settings may be obtained by a CPU Input instruction. The I/O address is specified in 2.22. Data Bits 4-7 contain the switch value; Bit 4 is the LSB of the switch. The ON position is binary 0.

Status Display and Switches

17.Ø The Status Display register provides signaling to a front panel mounted Light Emitting Diode (LED) display, and allows a variety of condition to be displayed to the system operator. The Status Display is controlled by CPU OUT instructions as outlined in 2.23.

17.1 Seven of the LED's, Data Bits Ø-6 corresponding to SL1-SL7, are general purpose and may be assigned on the faceplate by a plastic overlay. The eighth LED, Data Bit 7, signals the functional state of the TCB-1: OFF indicates no power, ON blinking indicates diagnostic status, and ON continuous indicates normal status. The Status Display will be set with LED's SL1-SL7 "ON", and SL8 blinking any time the CPU is being forced to exe- cute "NOP's" (i.e. the Processor is not operating). This occurs at Power-ON, normal exit from Diagnostic mode, and during Memory Parity Error execution suspension.

17.2 The display panel also provides two momentary contact switches, "DIS" signals the communication interface to inactivate the Data Terminal Ready signal and "RST" generates a Power-On Reset state.

Status Display Bits

17.3

Data Bit	Ø	1	2	3	4	5	6	7
Display LED	SL1	SL2	SL3	SL4	SL5	SL6	SL7	SL8
Binary 1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Binary Ø	ON	ON	ON	ON	ON	ON	ON	Blinking

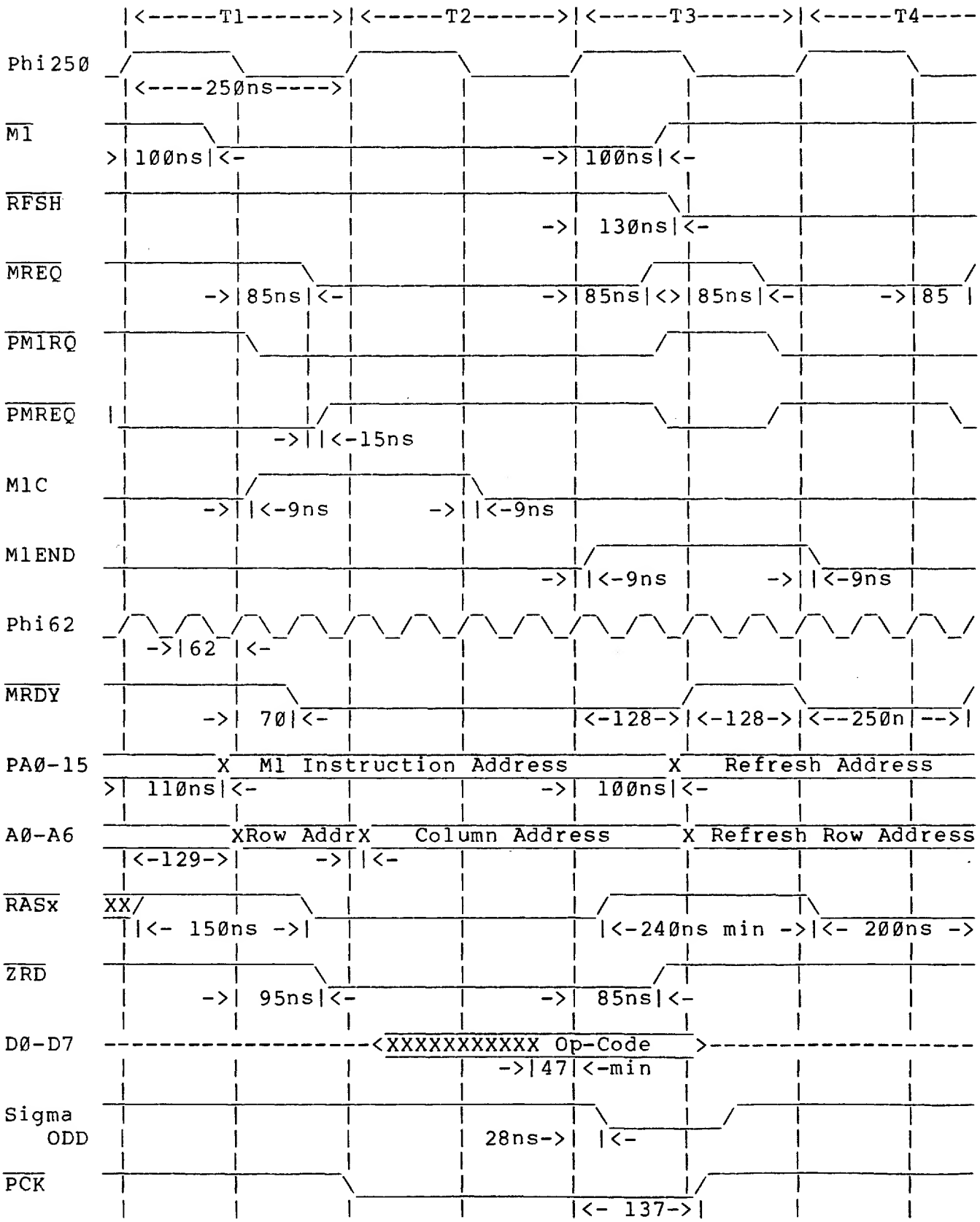
Telecommunication Processor

Timing Diagrams

The following diagrams indicates signal relationships for each section within the TCB-1. All signal names are capitol letters, Greek letters are spelled in English equivalents (i.e. Phi, Rho, Theta, Mu).

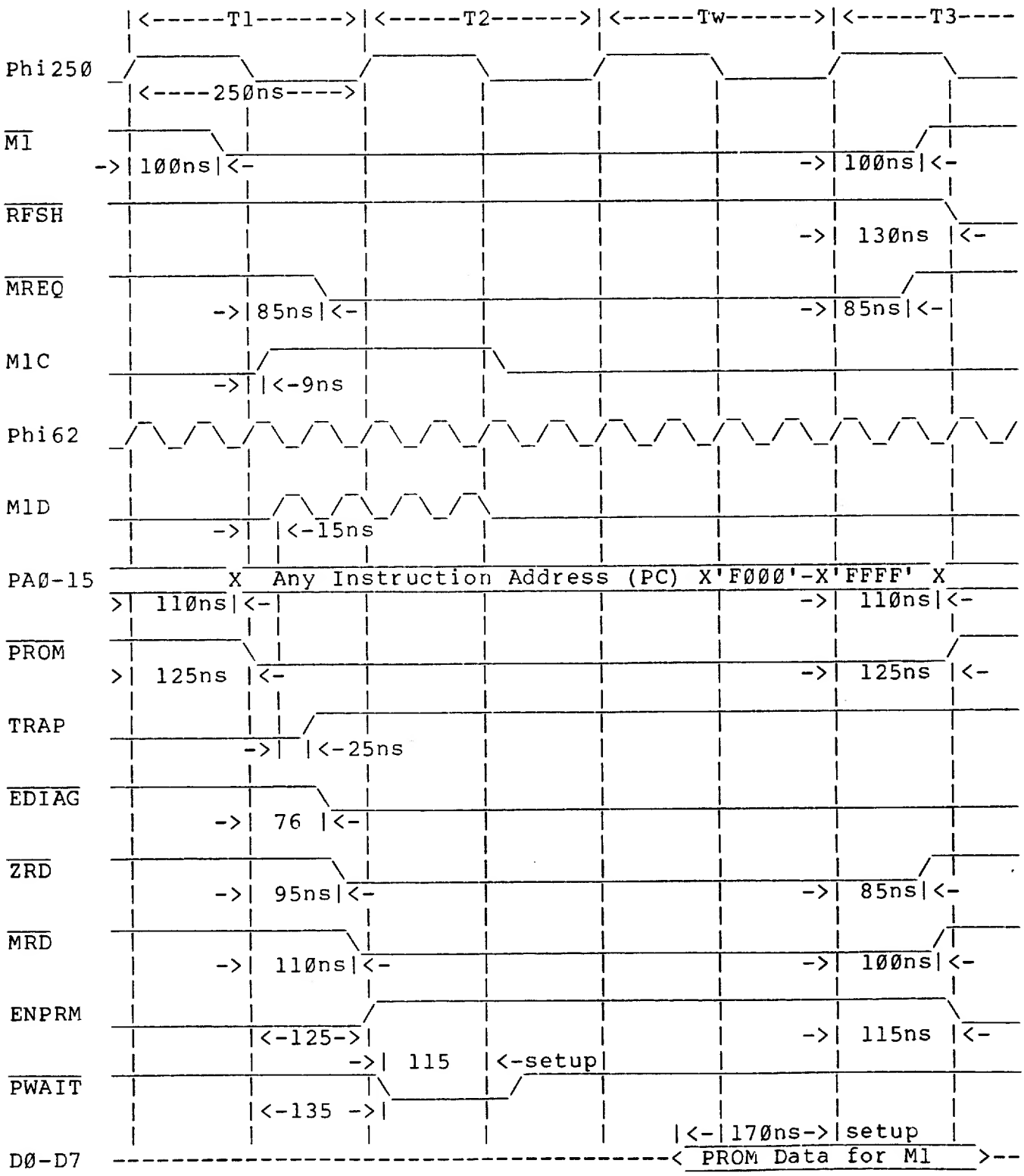
CPU M1 Cycle

Scale: 15.6ns/sp



CPU M1 Cycle from PROM

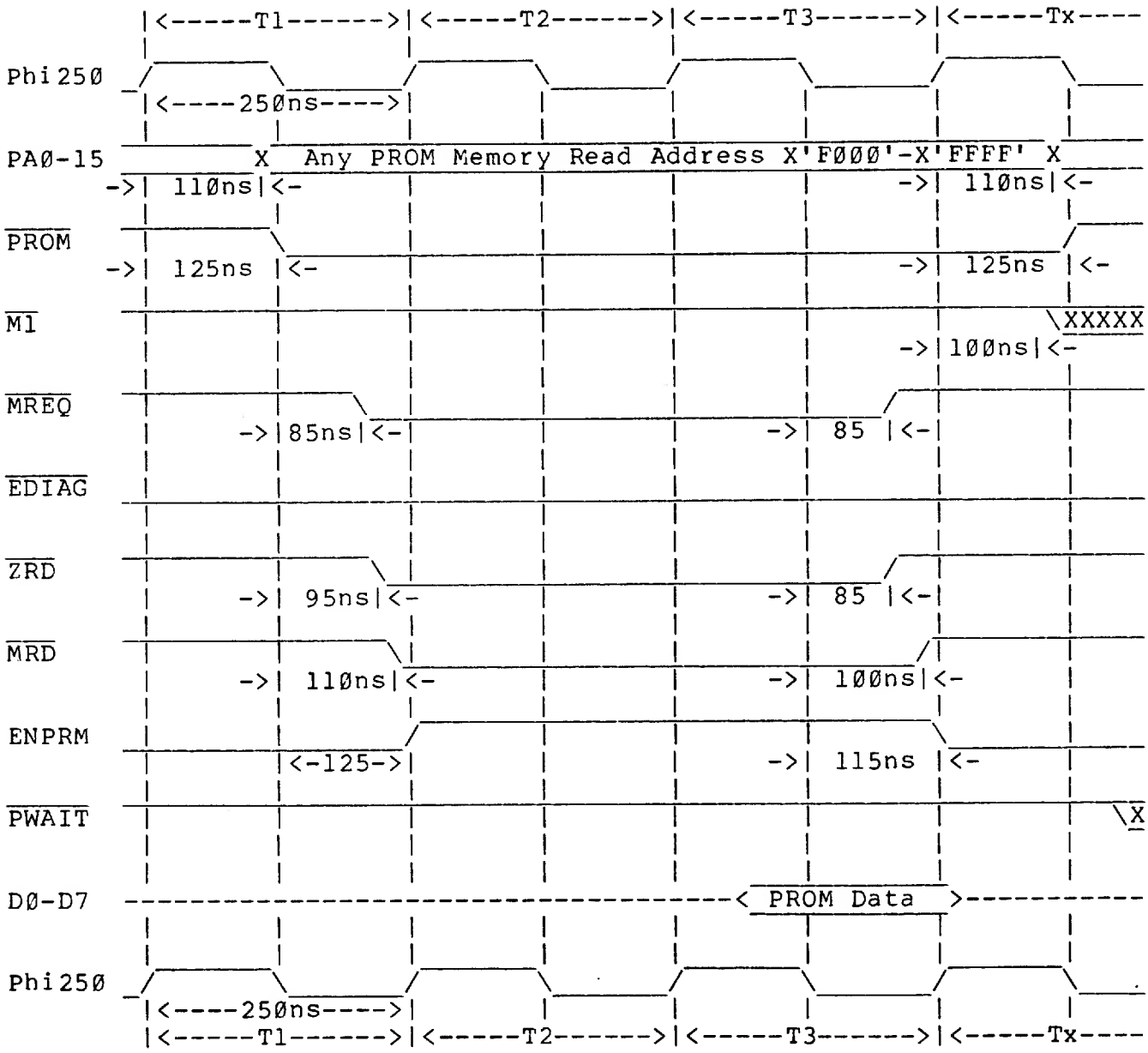
Scale: 15.62/ns



Note: $\overline{\text{RESET}}$, $\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, and $\overline{\text{WR}}$ are inactive (High).

CPU Read Cycle from PROM

Scale: 15.62/ns

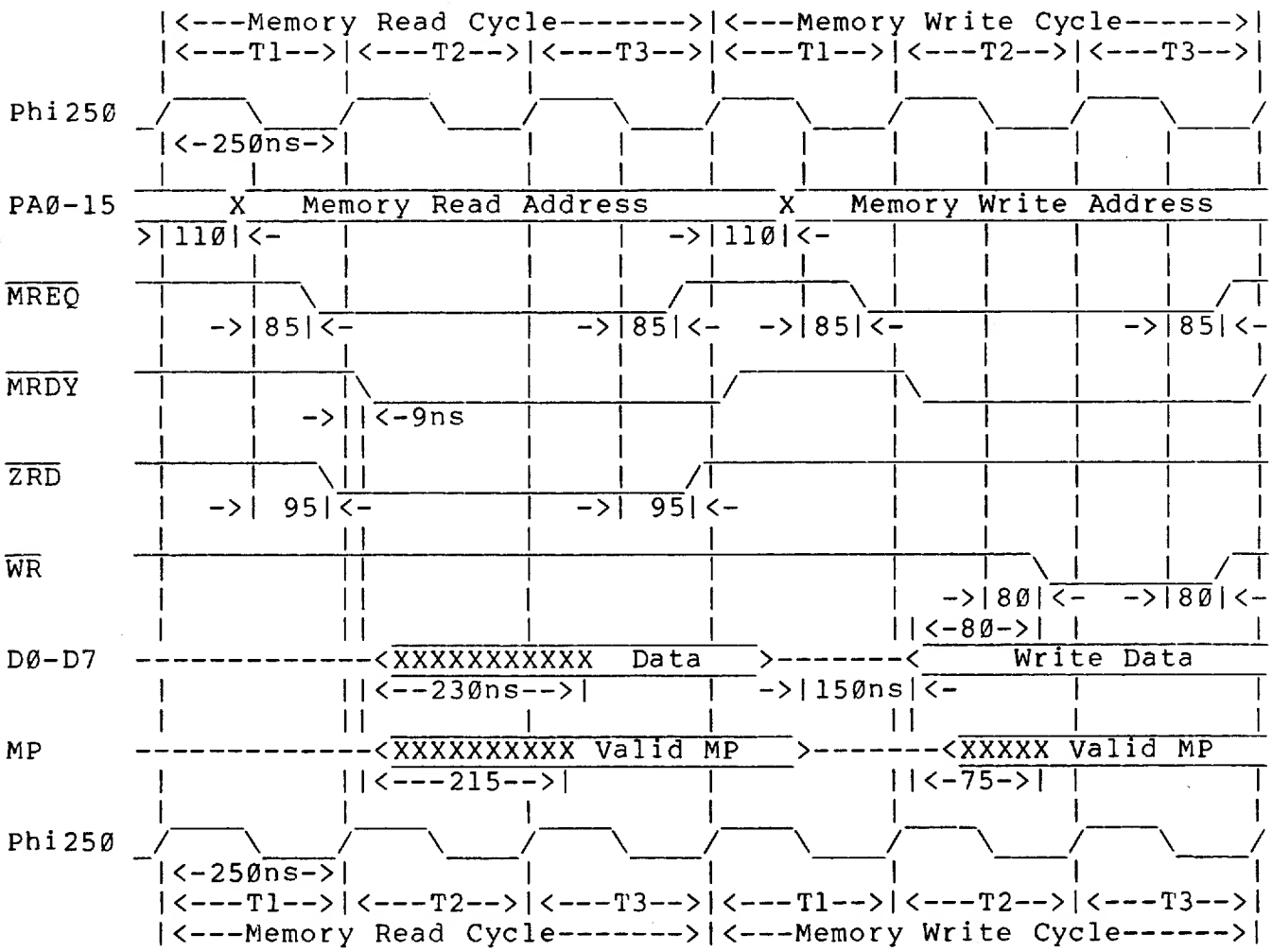


Note: RESET, BUSRQ, BUSAK INT, IORQ, M1, WR and RFSH are inactive.

CPU Memory Read and Write Cycle

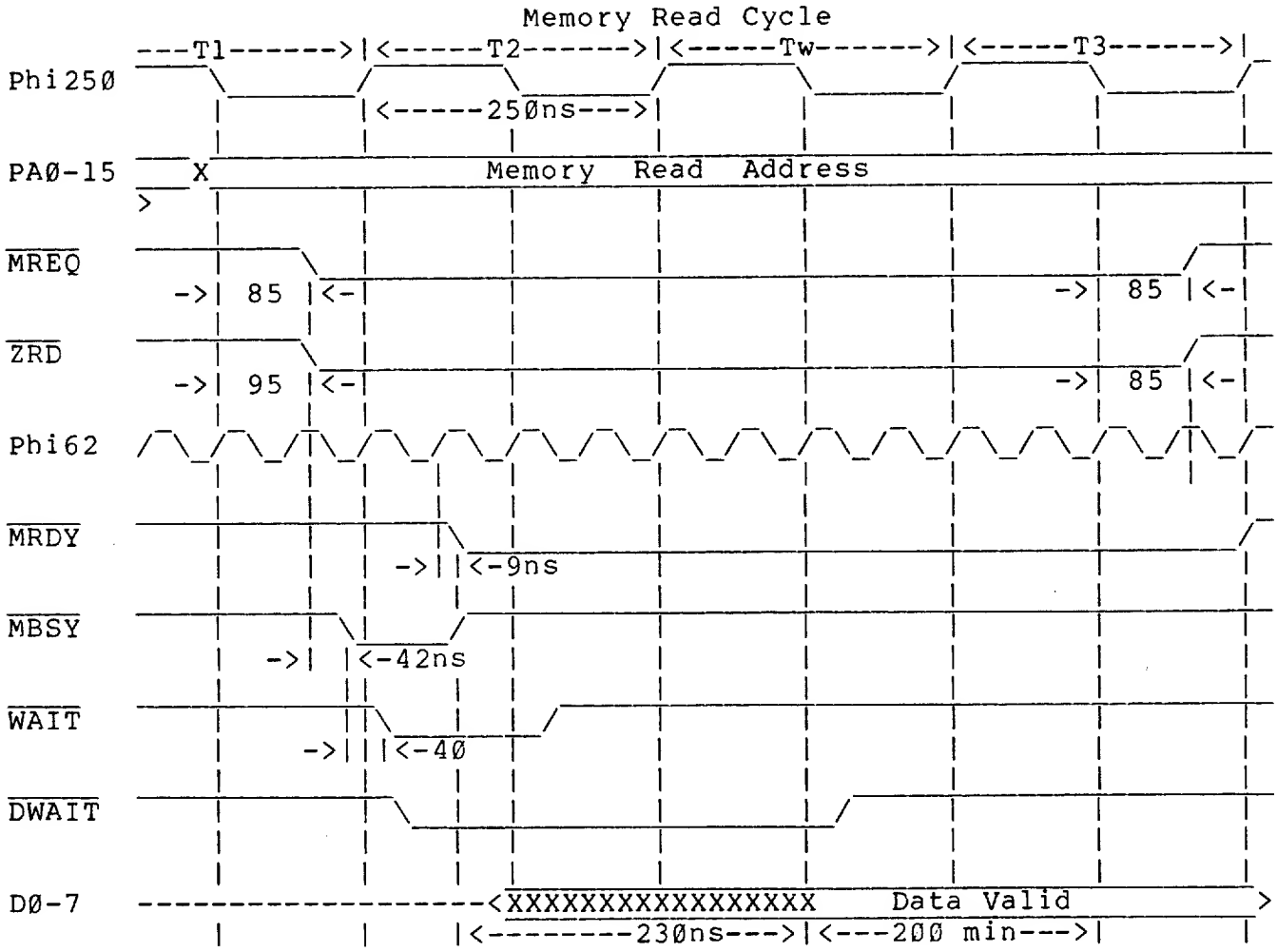
Scale: 25ns/sp

No memory contention.



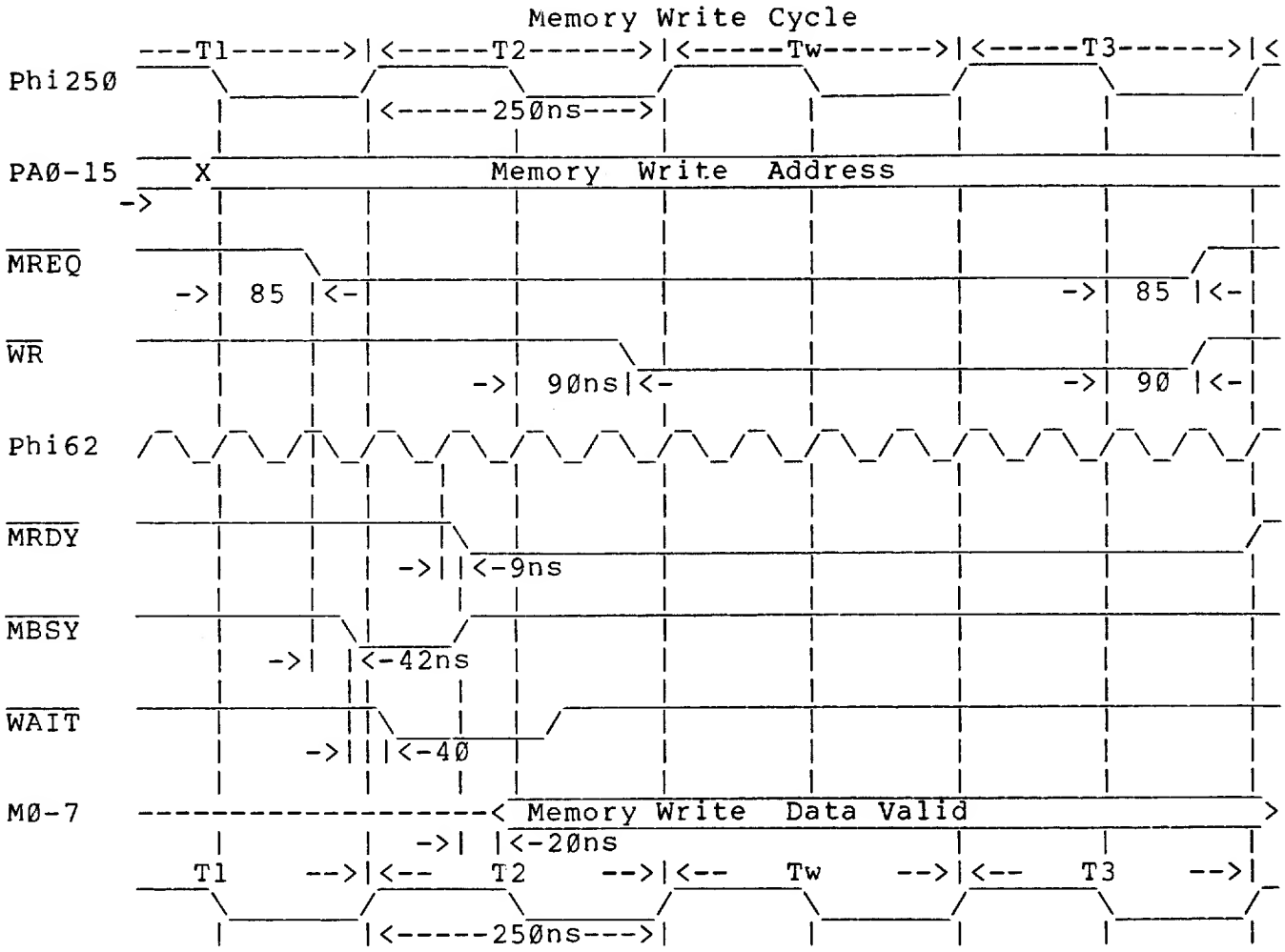
Note: $\overline{\text{RESET}}$,$\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ and $\overline{\text{RFSH}}$ are inactive (High).

CPU Memory Read Cycle
With Memory Contention
Scale: 15.6ns/sp



Note: $\overline{\text{RESET}}$,$\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, $\overline{\text{M1}}$, $\overline{\text{WR}}$ and $\overline{\text{RFSH}}$ are inactive.

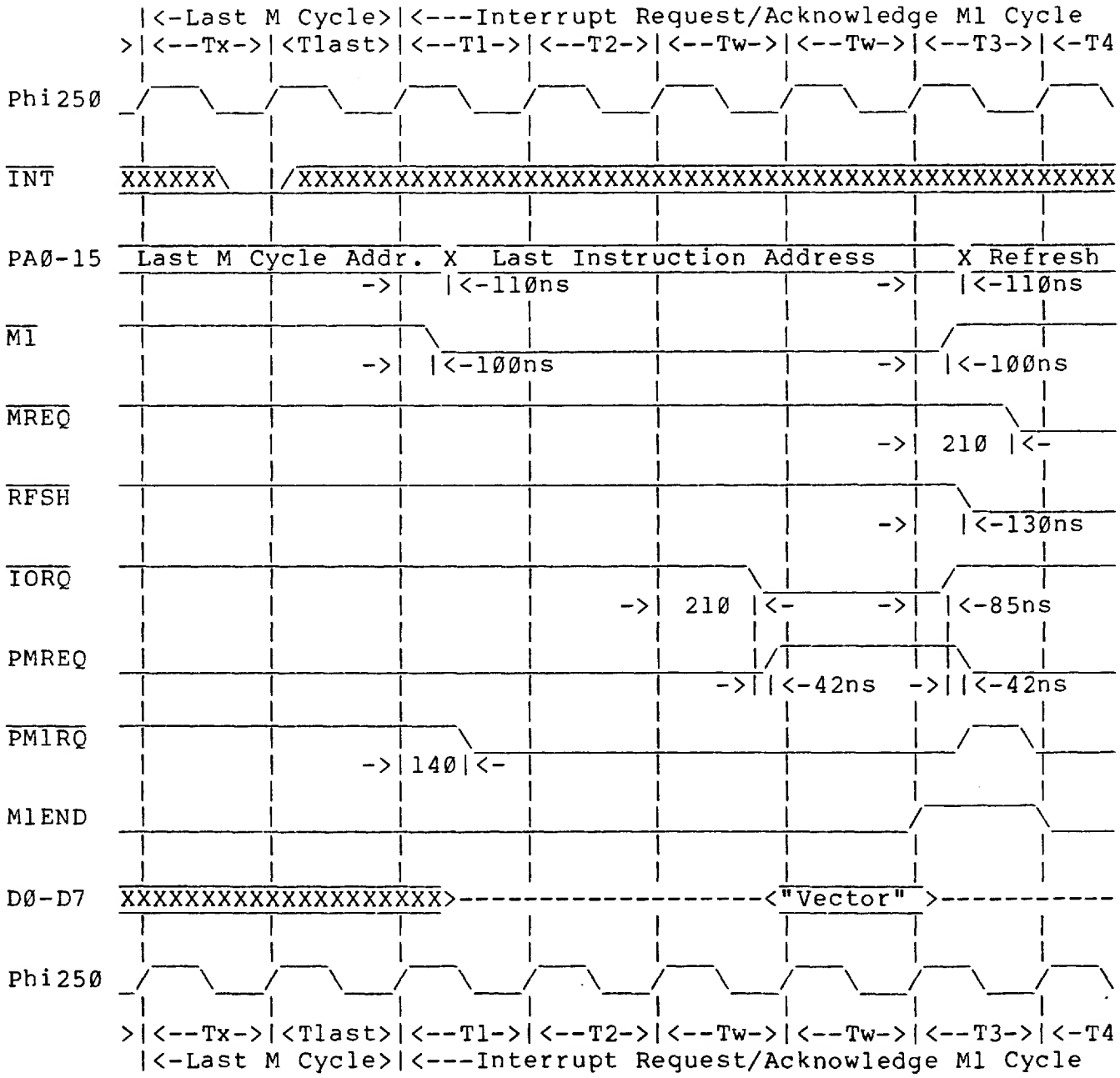
CPU Memory Write Cycle
With Memory Contention
Scale: 15.6ns/sp



Note: $\overline{\text{RESET}}$,$\overline{\text{BUSRQ}}$, $\overline{\text{BUSAK}}$ $\overline{\text{INT}}$, $\overline{\text{IORQ}}$, $\overline{\text{M1}}$, $\overline{\text{RD}}$ and $\overline{\text{RFSH}}$ are inactive.

CPU Interrupt Request/Acknowledge Cycle

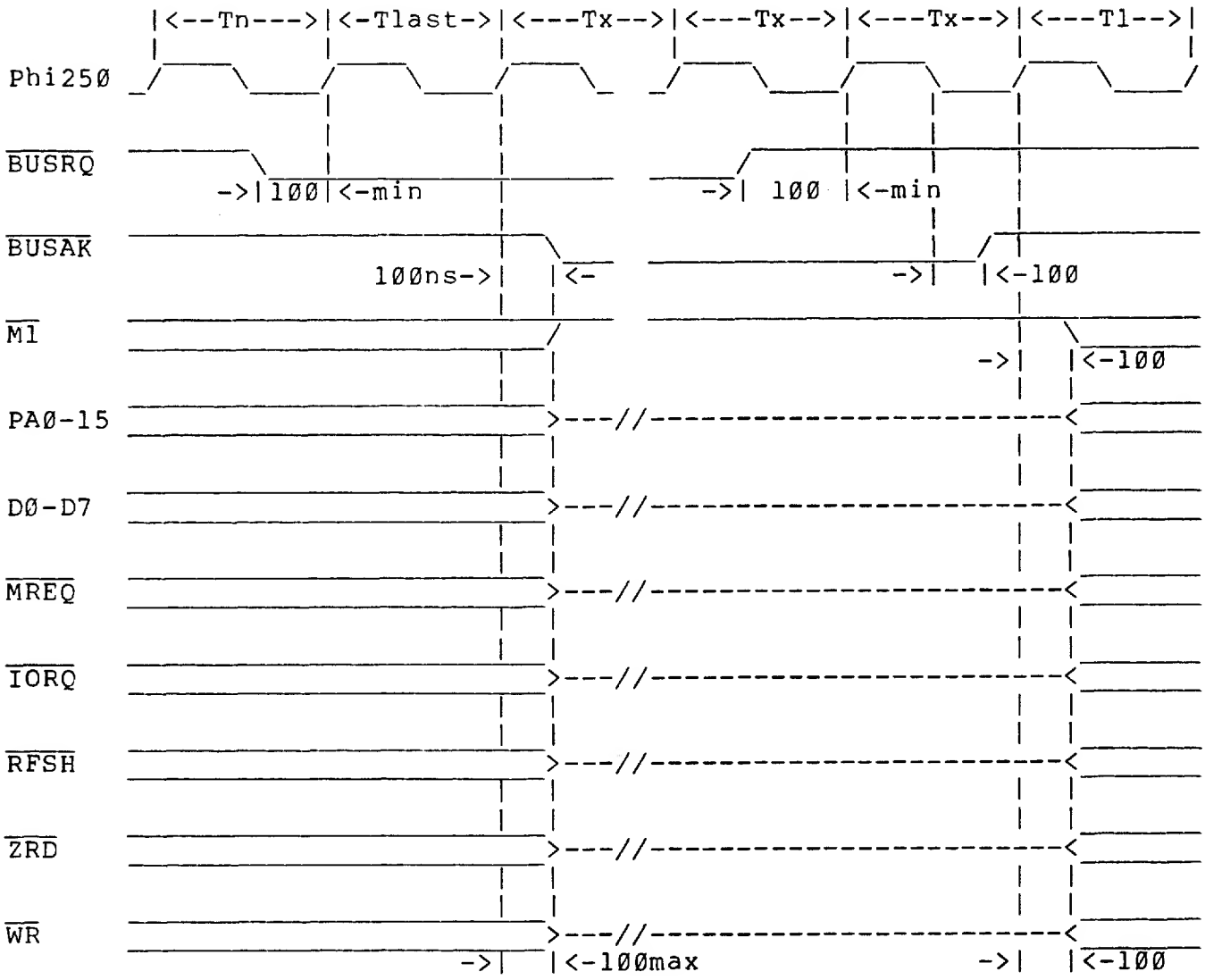
Scale 31.25ns/sp



Note: RESET, BUSRQ, BUSAK ZRD, and WR are inactive (High).

CPU Bus Request/Acknowledge Cycle

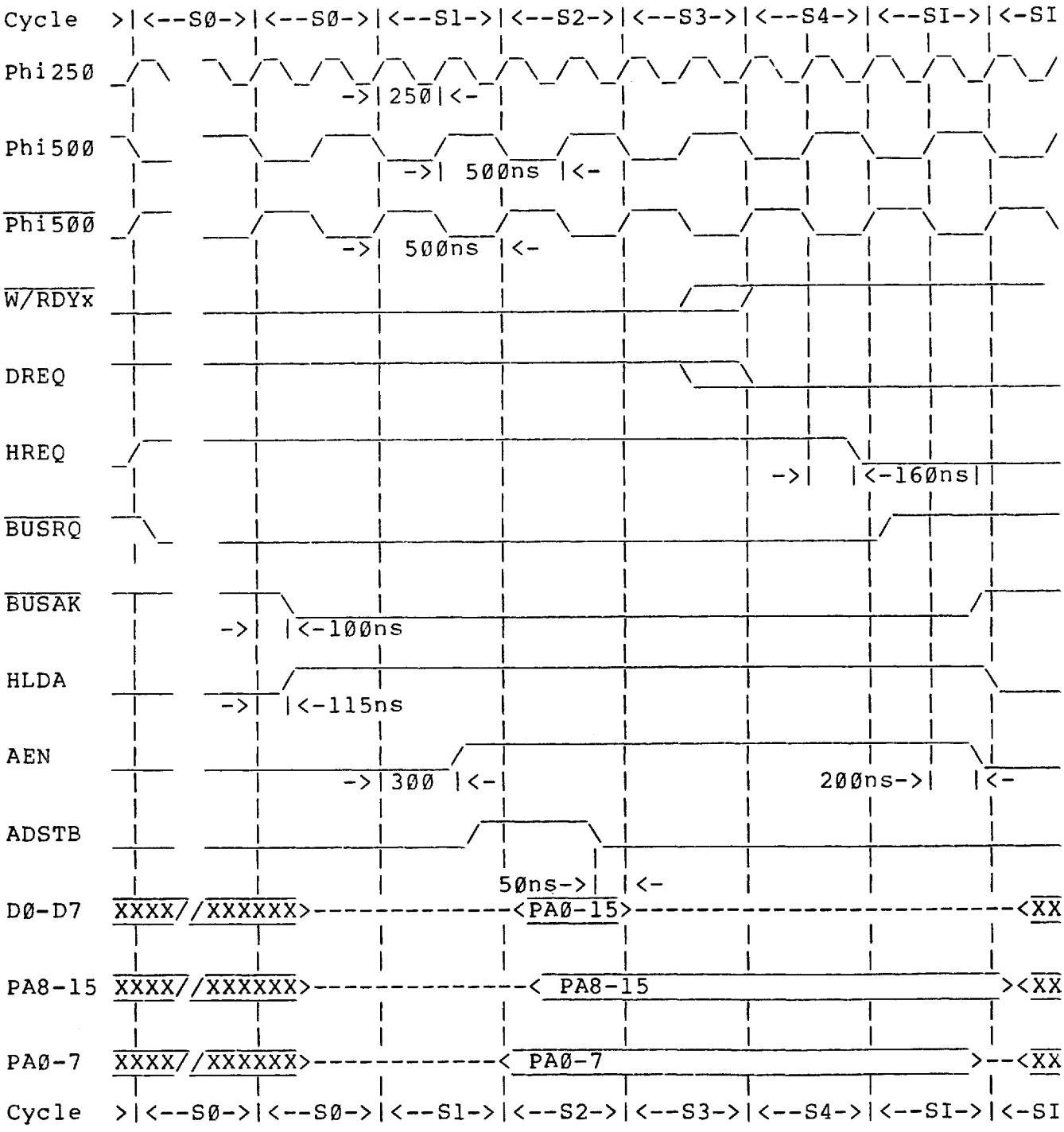
Scale: 25ns/sp



9517A-DMA Controller

Bus Control

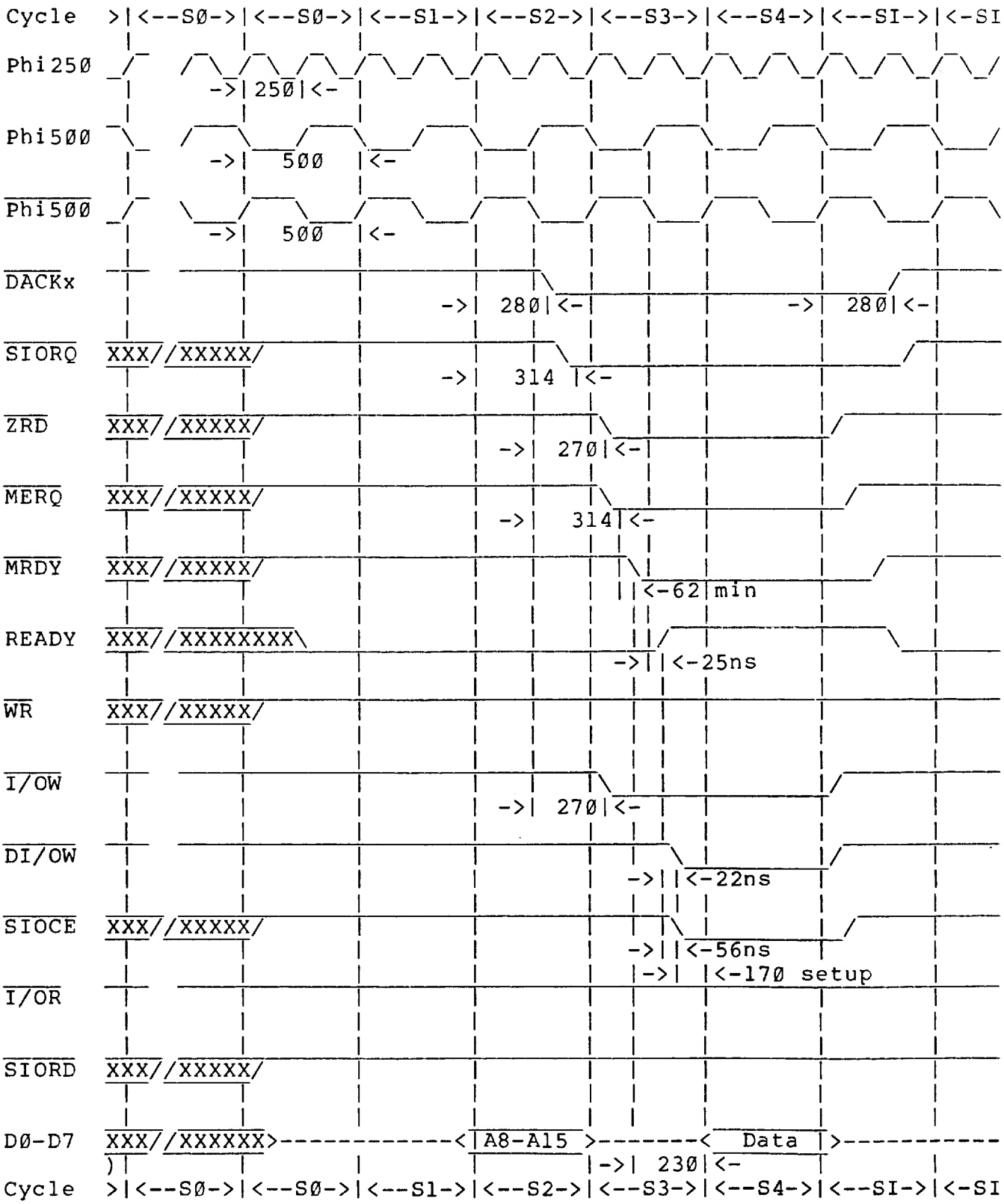
Scale: 62ns/sp



9517-DMA Controller (con't)

Data from Memory to SIO/2

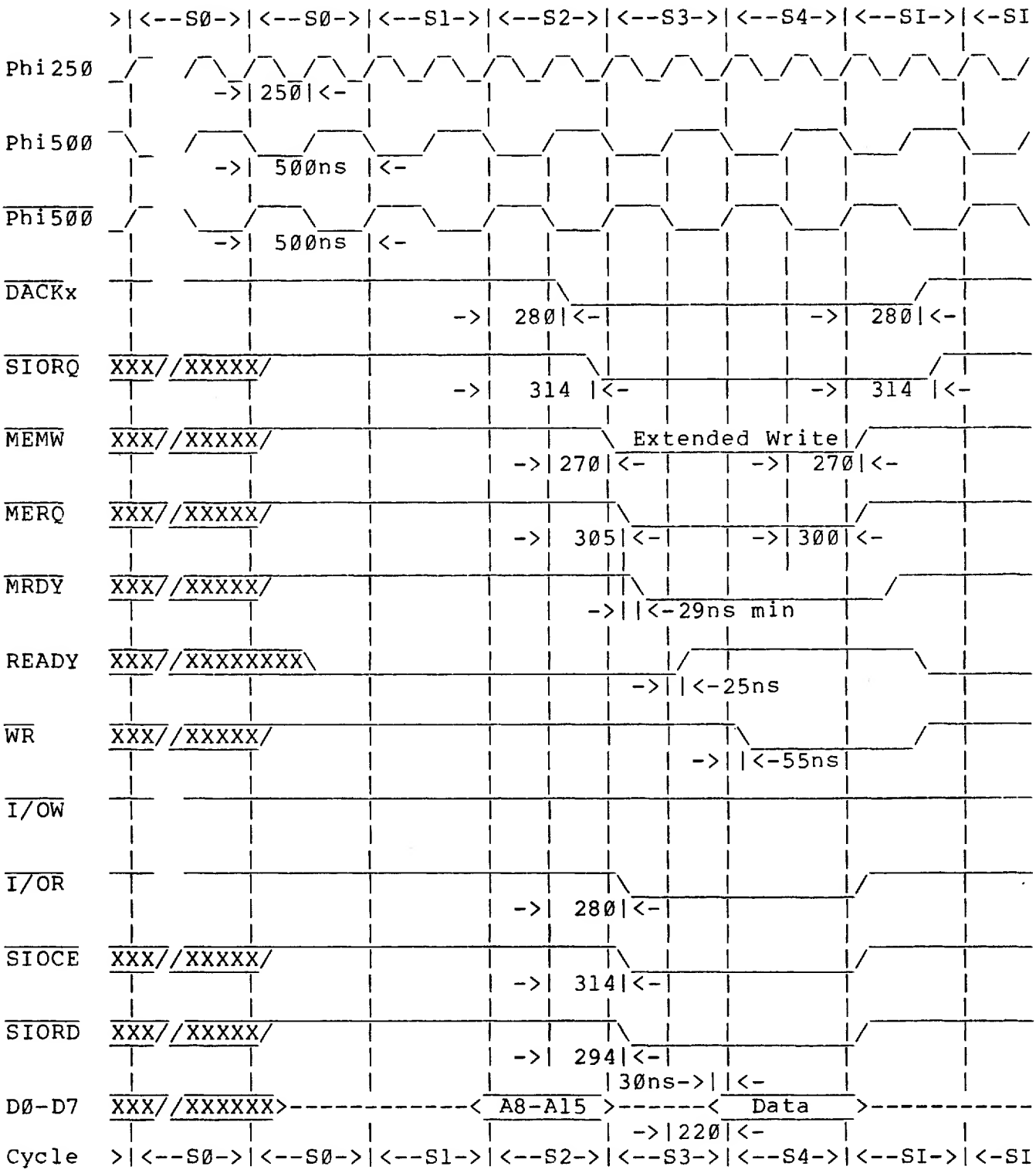
Scale: 62.5ns/sp



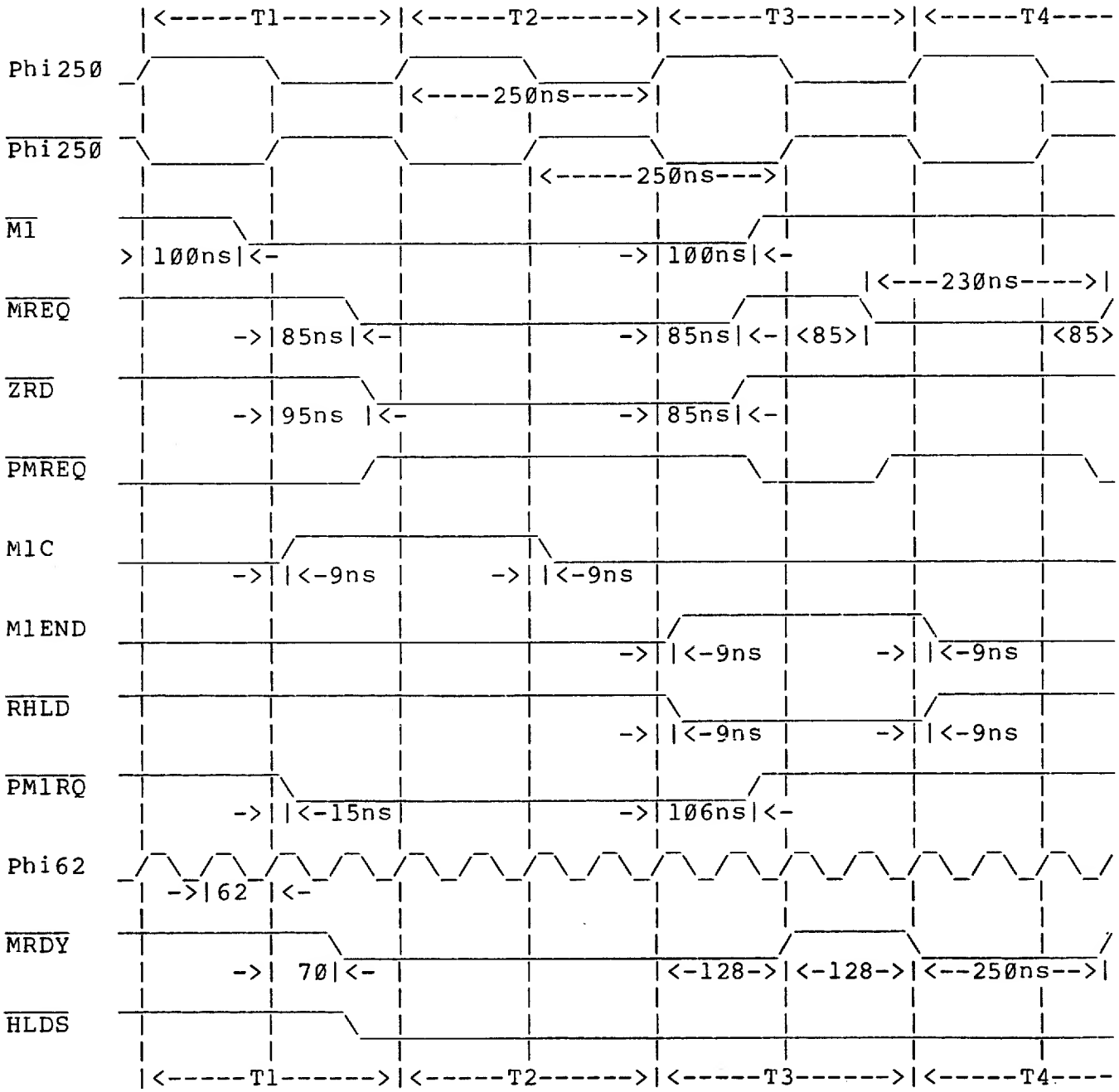
9517-DMA Controller (con't)

Data from SIO/2 to Memory

Scale: 62.5ns/sp



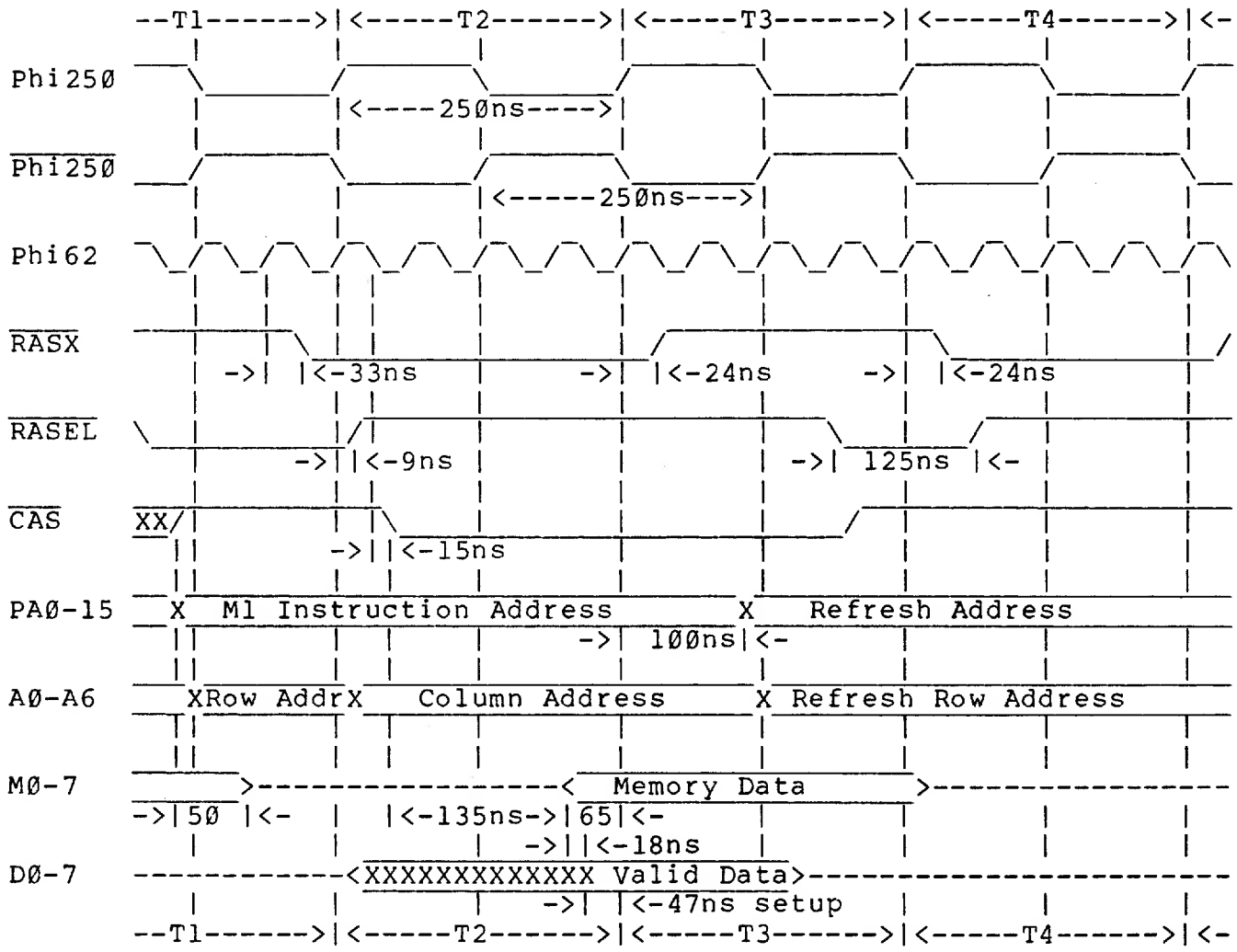
Memory Controller
CPU M1 Cycle Request
Scale: 15.6ns/sp



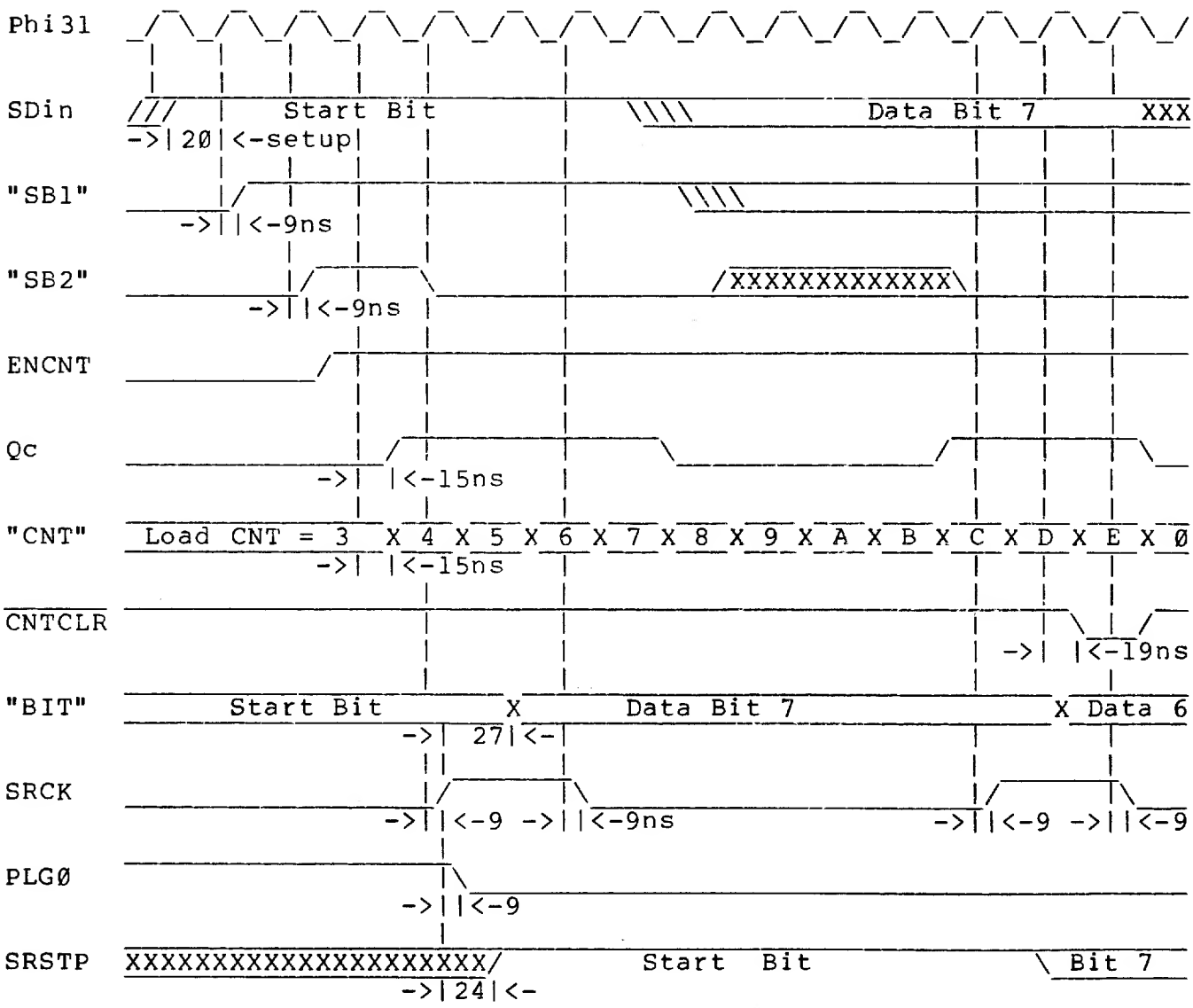
Memory Controller con't.

CPU M1 Cycle Request

Scale: 15.6ns/sp



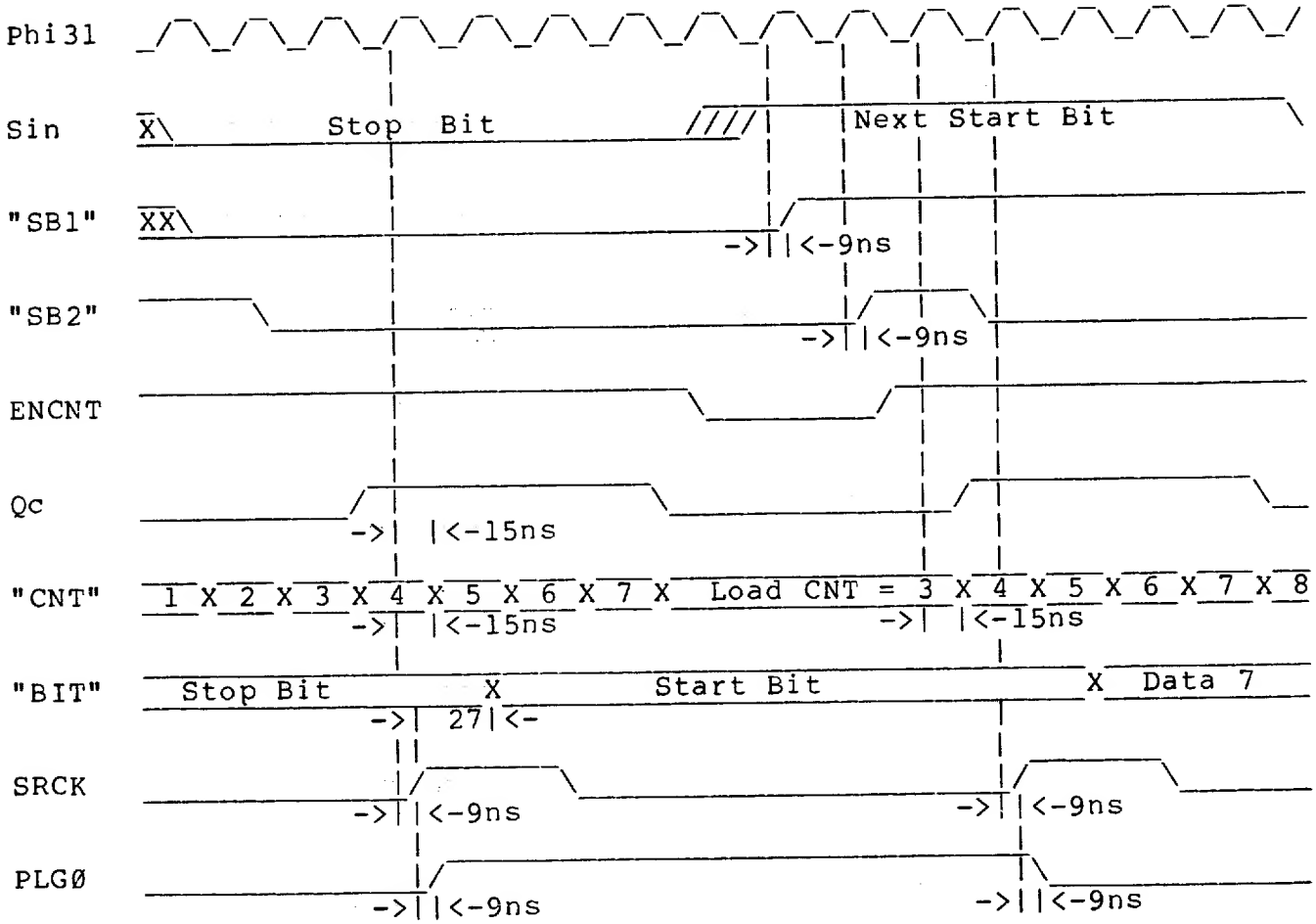
928 Data Link
Receiver Start Bit Synchronization
Scale: 7.83ns/sp



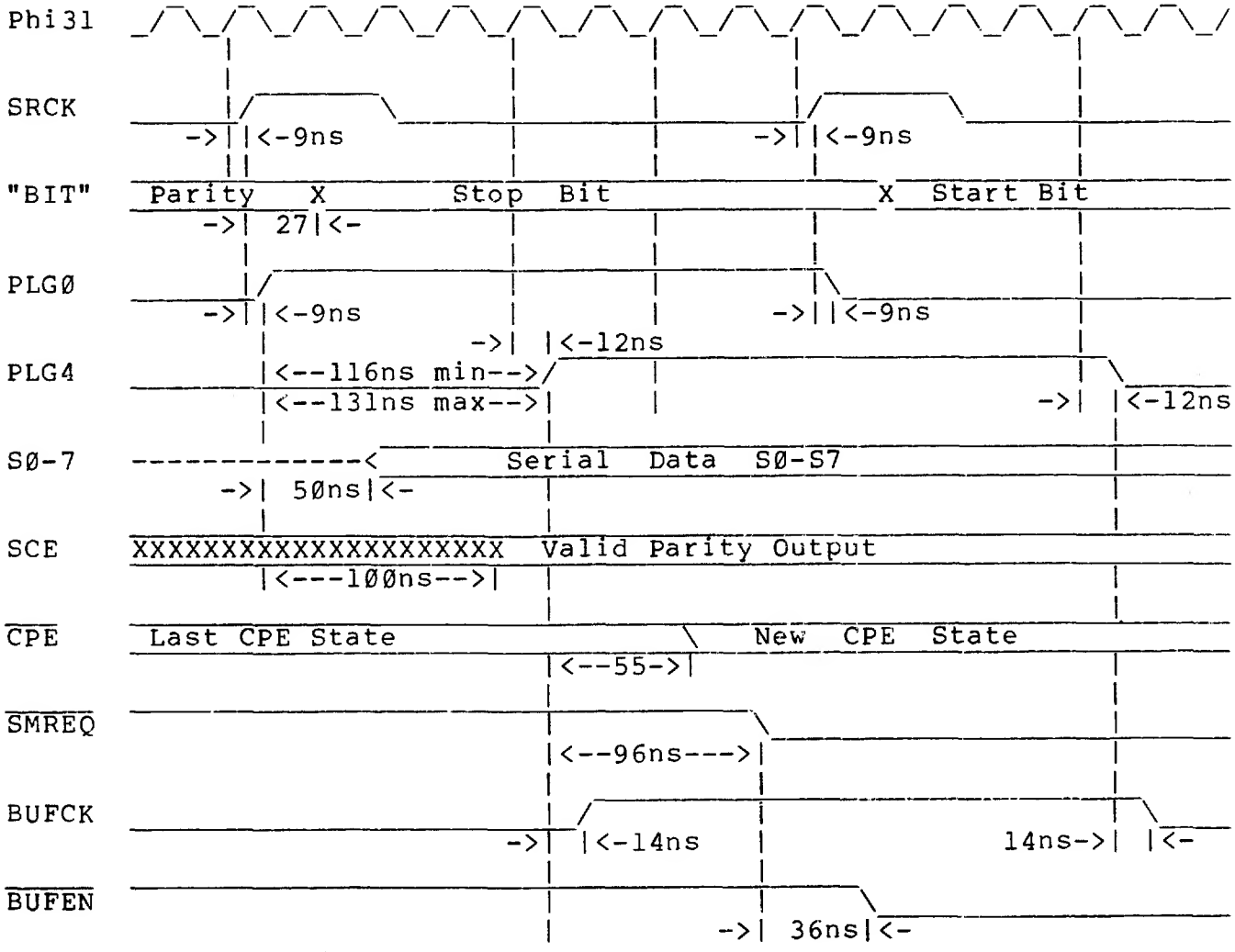
928 Data Link

Receiver Stop/Start Bit Synchronization

Scale: 7.83ns/sp



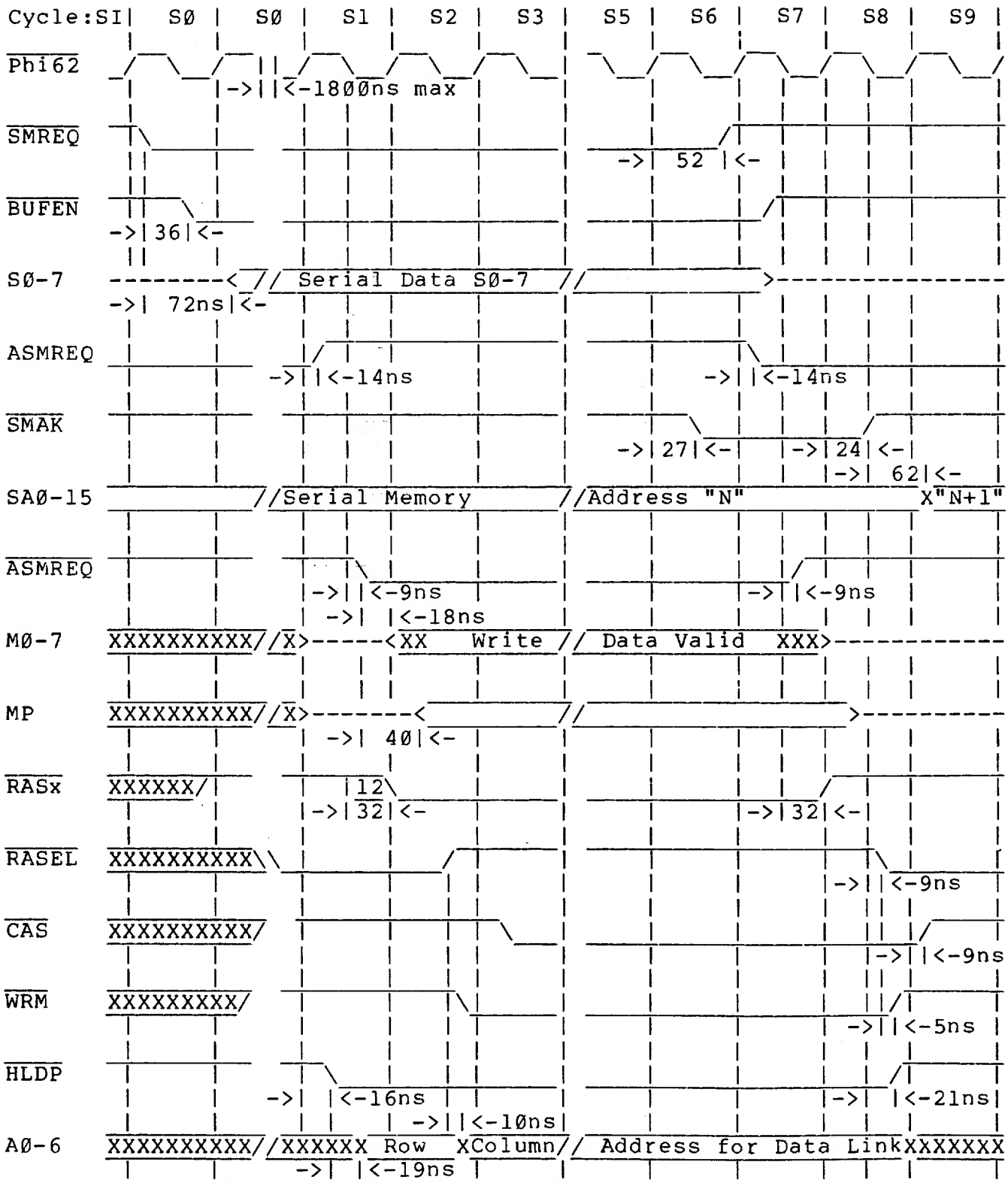
928 Data Link Receiver
Double Buffer Timing
Scale: 7.83/sp



928 Data Link Memory Interface

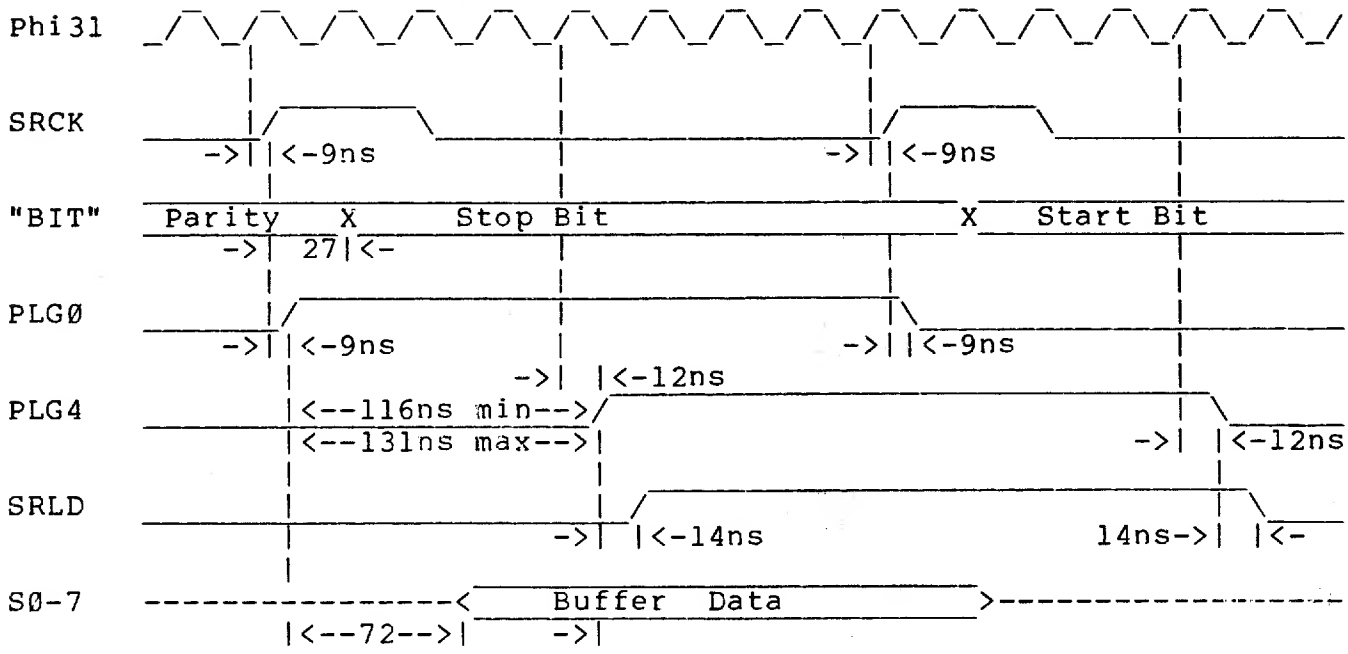
Write Timing

Scale: 10.4ns/sp



Note: MWT = 1, SWR = 0, and TRANS = 0.

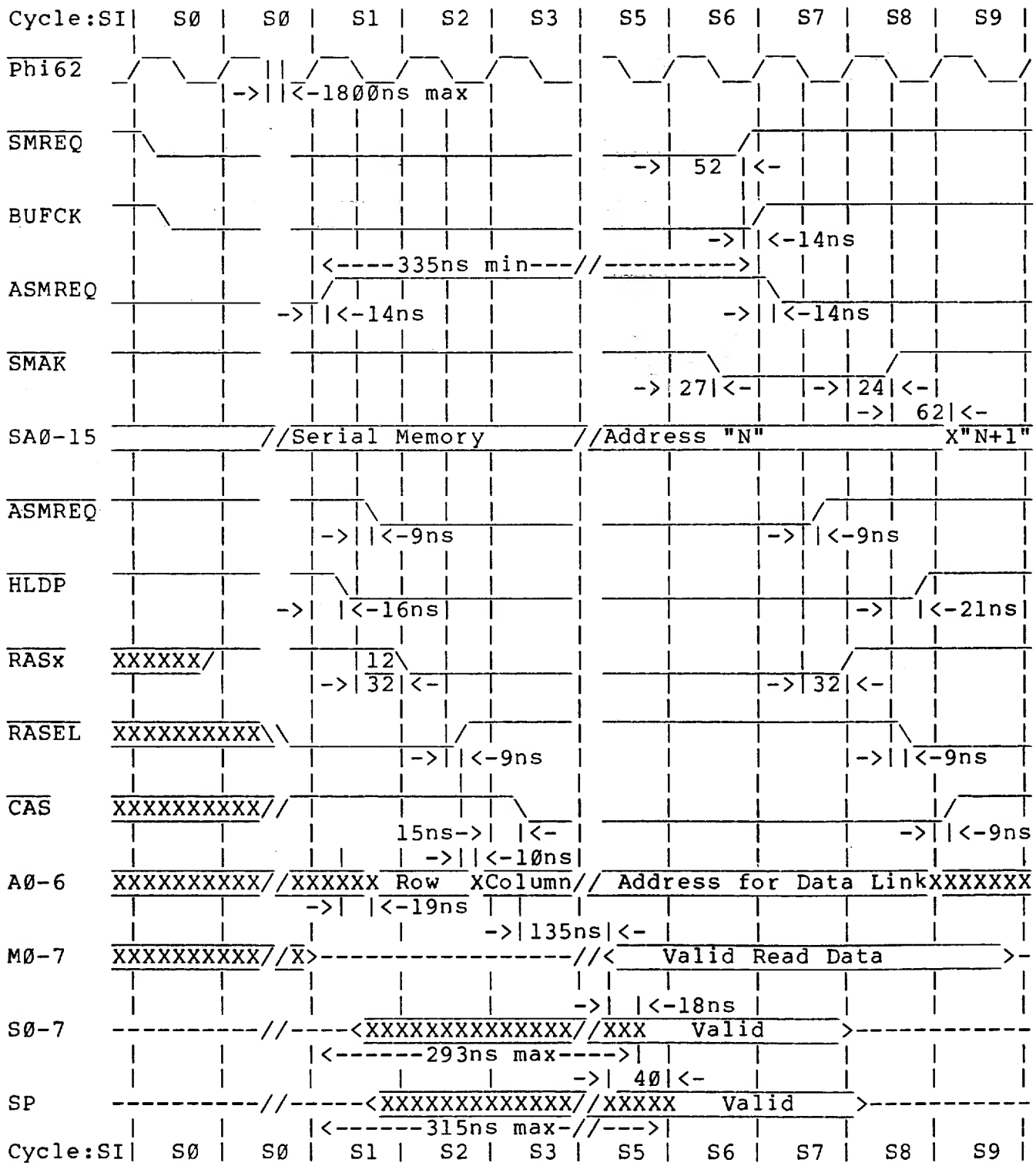
928 Data Link Transmitter
Double Buffer Timing
Scale: 7.83/sp



928 Data Link Memory Interface

Read Timing

Scale: 10.4ns/sp.



Note: MWT = 0, $\overline{SWR}$ = 1, and TRANS = 1.

928 Data Link B1 State Timing
Scale 7.83ns/sp